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## N-CHANNEL POWER MOS FET ARRAY SWITCHING TYPE

### DESCRIPTION

The μPA1501 is N-channel Power MOS FET Array that built in 4 circuits and surge absorber designed for solenoid, motor and lamp driver.

### FEATURES

- 4 V driving is possible
- Low On-state Resistance  
 $R_{DS(on)} \leq 0.42 \Omega$  MAX. ( $V_{GS} = 10 V, I_D = 2 A$ )  
 $R_{DS(on)} \leq 0.49 \Omega$  MAX. ( $V_{GS} = 4 V, I_D = 2 A$ )
- Surge Absorber, built in.

### ORDERING INFORMATION

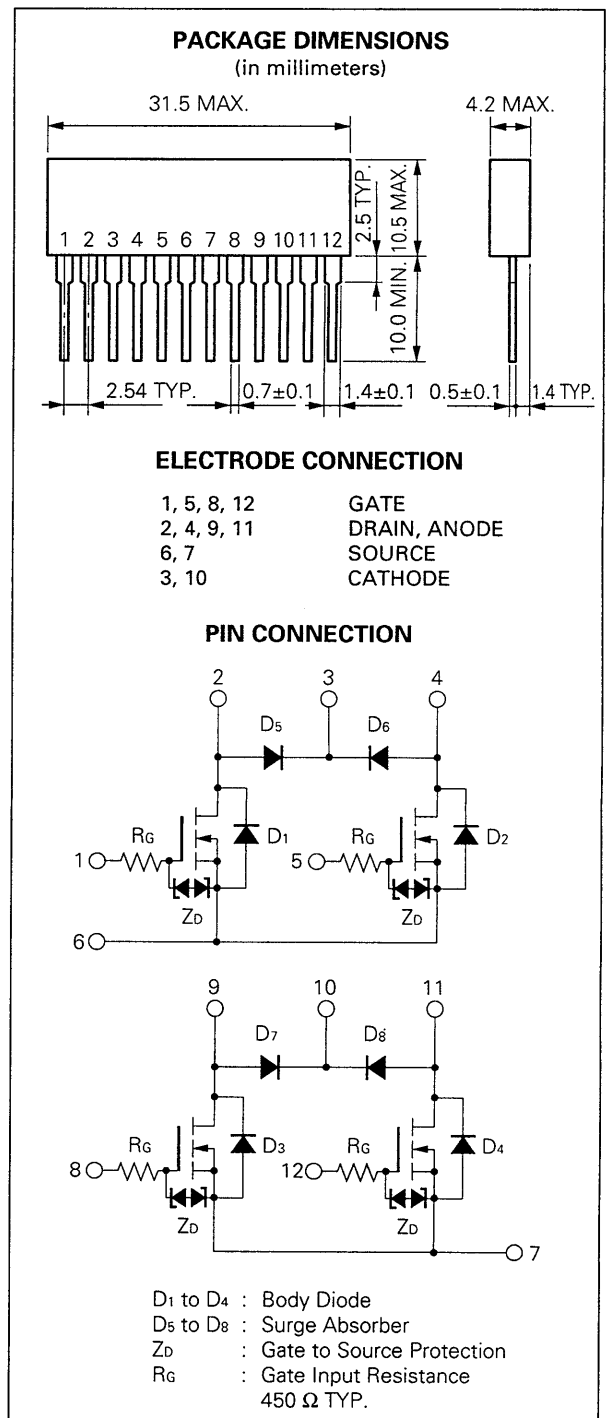
Part Number	Package	Quality Grade
μPA1501H	12-Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

Drain to Source Voltage	$V_{DSS}$	120	V
Gate to Source Voltage	$V_{GSS(AC)}$	+20, -10	V
Drain Current (DC)	$I_{D(DC)}$	±3.0	A/unit
Drain Current (pulse)	$I_{D(pulse)*}$	±12	A/unit
Repetitive Peak Reverse Voltage	$V_{RRM}$	140	V
Diode Forward Current	$I_{F(AV)}$	3.0	A/unit
Total Power Dissipation (4 circuits)	$P_T$	4.0	W
< $T_a = 25^\circ C$ >			
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$



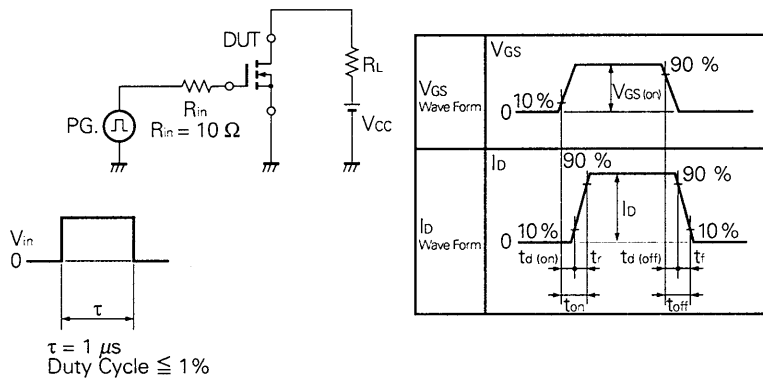
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±10 V, V <sub>DS</sub> = 0
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	2.2			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2 A
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>		0.42	0.55	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A
Drain to Source On-state Resistance	R <sub>DS(on)2</sub>		0.49	0.65	Ω	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 2 A
Input Capacitance	C <sub>iss</sub>		620		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1.0 MHz
Output Capacitance	C <sub>oss</sub>		140		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		10		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		75		ns	I <sub>D</sub> = 2 A V <sub>GS</sub> = 10 V V <sub>DD</sub> = 30 V R <sub>L</sub> = 15 Ω See Fig. 1
Rise Time	t <sub>r</sub>		60		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		900		ns	
Fall Time	t <sub>f</sub>		200		ns	
Total Gate Charge	Q <sub>G</sub>		13		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 3 A V <sub>DD</sub> = 48 V See Fig. 2
Gate to Source Charge	Q <sub>GS</sub>		3		nC	
Gate to Drain Charge	Q <sub>GD</sub>		2		nC	

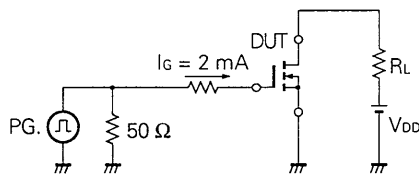
**SURGE ABSORBER (Diode, built in) 1 Unit**

Repetitive Peak Reverse Current	I <sub>RRM</sub>			10	μA	V <sub>R</sub> = 140 V
Diode Forward Voltage	V <sub>F</sub>		1.2		V	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0

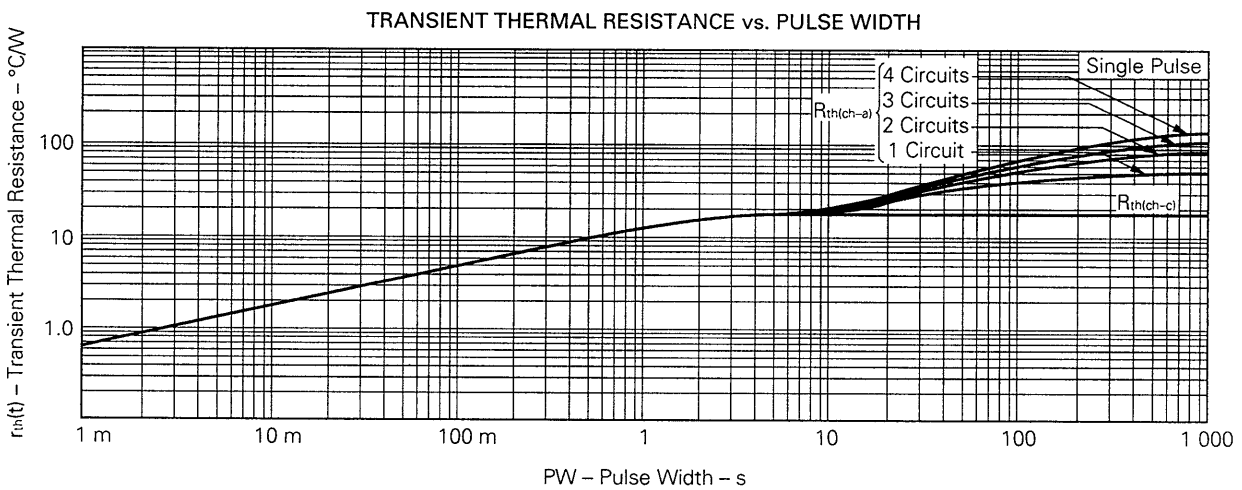
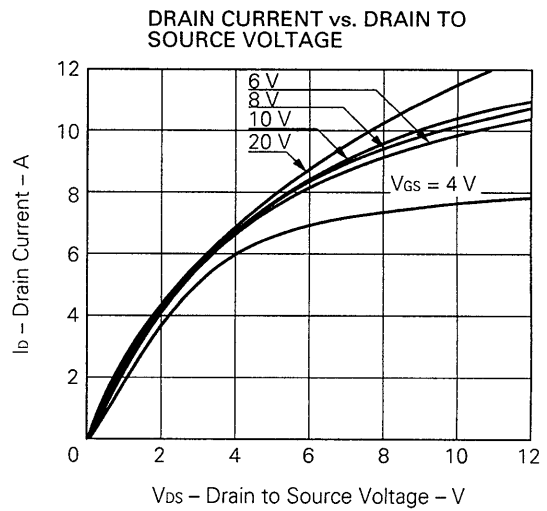
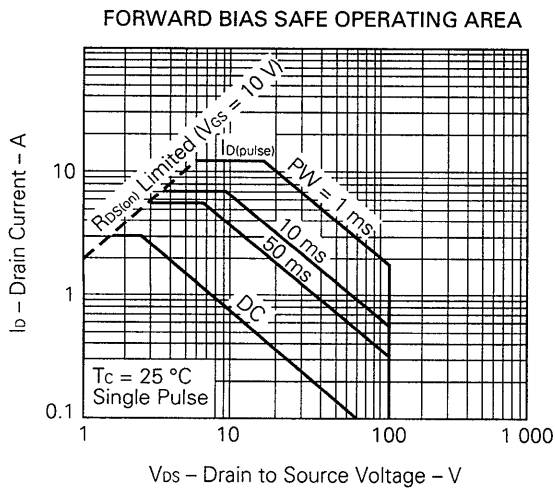
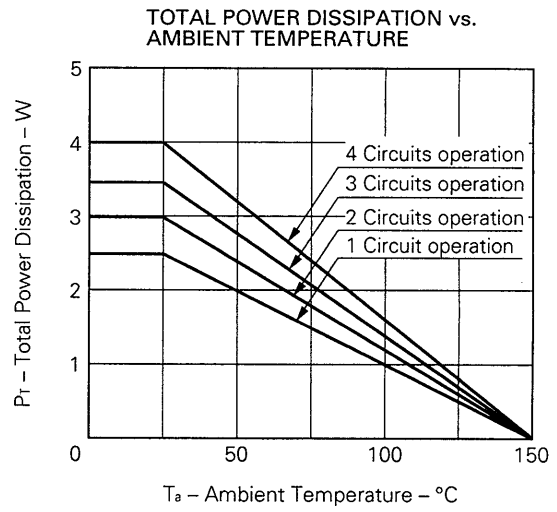
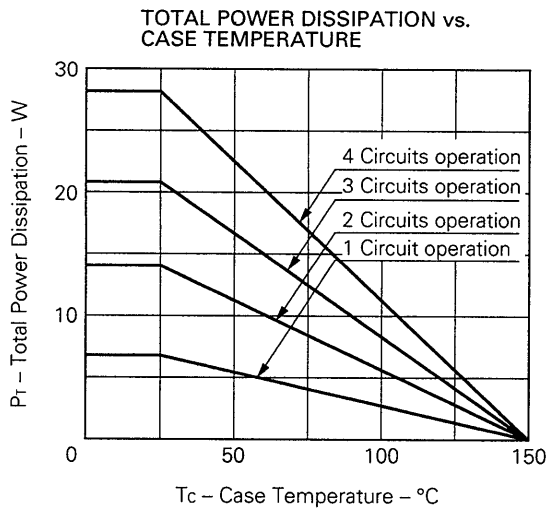
**Fig. 1 Switching Test Circuit**



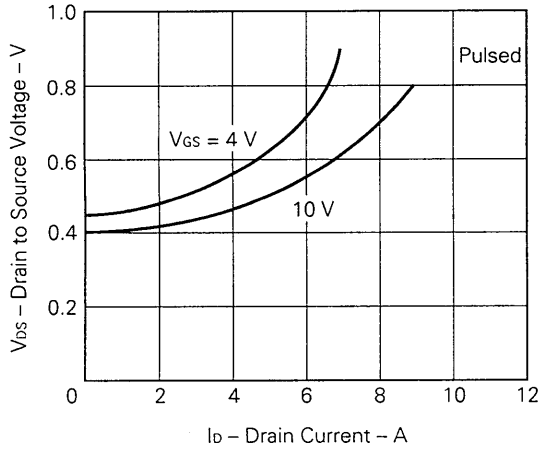
**Fig. 2 Gate Charge Test Circuit**



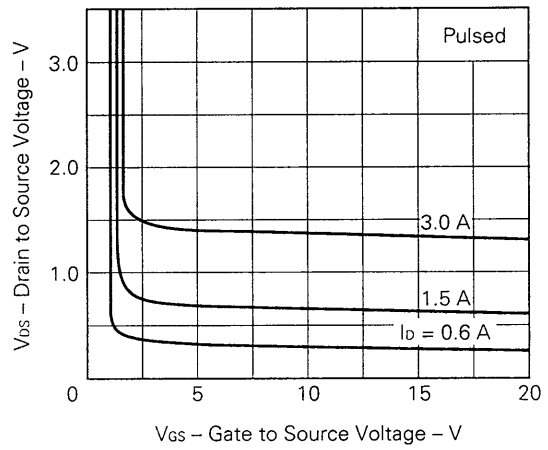
TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )



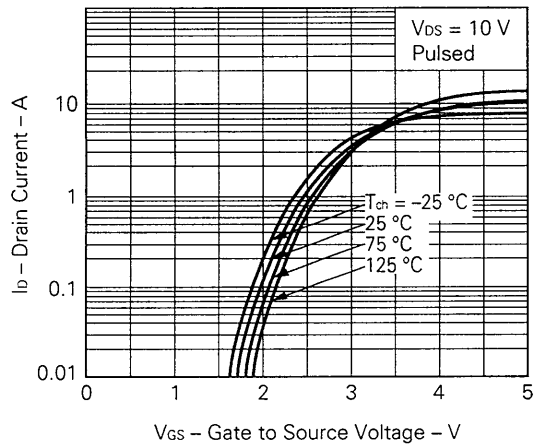
DRAIN TO SOURCE VOLTAGE vs. DRAIN CURRENT



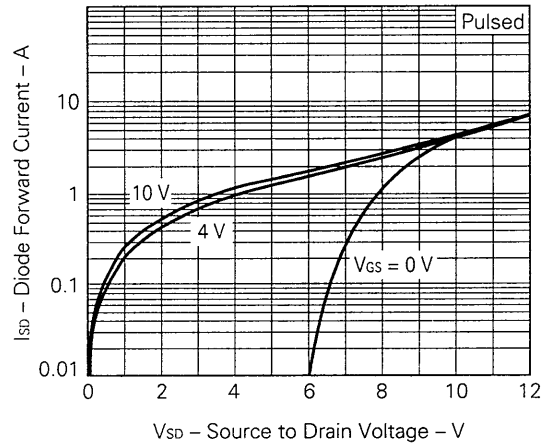
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE



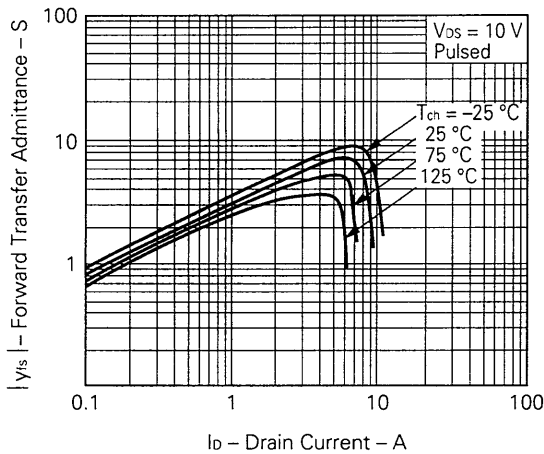
TRANSFER CHARACTERISTIC



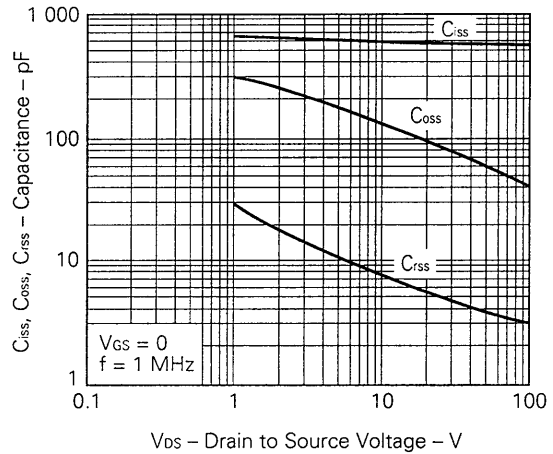
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



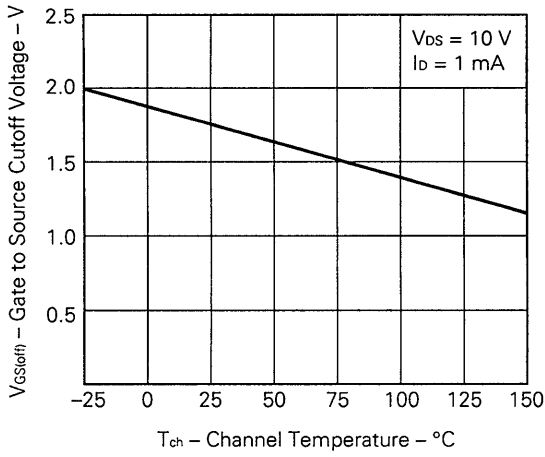
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



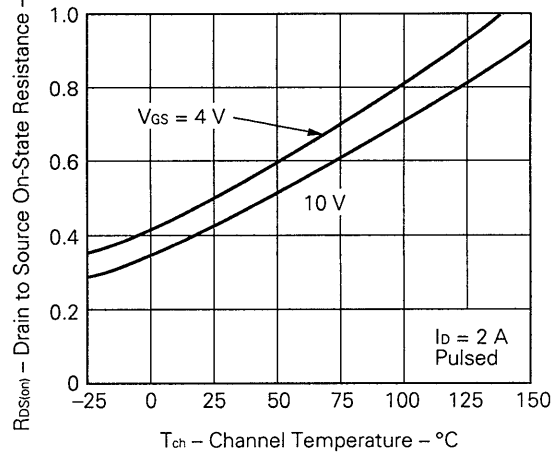
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



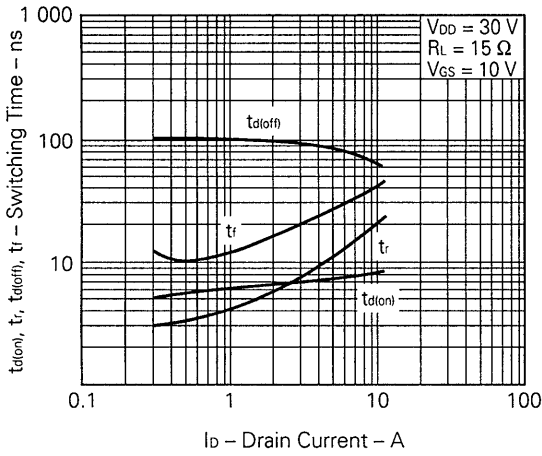
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



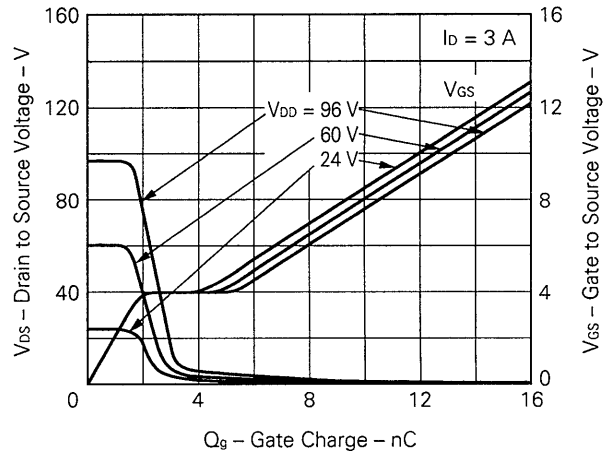
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



SWITCHING TIME vs. DRAIN CURRENT



DYNAMIC INPUT CHARACTERISTIC



**Reference**

Application note name	No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Application circuit using Power MOS FET	TEB-1035

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