

The TDS5 is a low voltage, high current, thin pack disc SCR employing a amplifying gate structure. This thin package provides greater cooling thus maximizing high current performance. The amplifying gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I²t Ratings

APPLICATIONS:

- DC Power Supplies
- Motor Controls
- Plating Rectifiers

ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.
 EXAMPLE: TDS520503DH is a 2000V-5000A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating I_{tavg}	Current Code	Turn-Off T_q	Gate I_{GT}	Leads
TDS5	2000	20	5000	50	0	3	DH
	1800	18					
	1600	16			500us	200ma	12"
	1400	14			(typ.)	(max)	
	1200	12					

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	2000	Volts
Average On-State Current, $T_C=68^\circ\text{C}$	$I_{T(Avg.)}$	5000	A
RMS On-State Current, $T_C=68^\circ\text{C}$	$I_{T(RMS)}$	7854	A
Average On-State Current, $T_C=55^\circ\text{C}$	$I_{T(Avg.)}$	5700	A
RMS On-State Current, $T_C=55^\circ\text{C}$	$I_{T(RMS)}$	8954	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	I_{TSM}	90,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	I_{TSM}	84,852	A
Fuse Coordination I^2t , 60Hz	I^2t	3.38E+07	A^2s
Fuse Coordination I^2t , 50Hz	I^2t	3.60E+07	A^2s
Critical Rate-of-Rise of On-State Current	di/dt	100	A/us
Repetitive			
Critical Rate-of-Rise of On-State Current	di/dt	300	A/us
Non-Repetitive			
Peak Gate Power, 100us	P_{GM}	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	T_j	-40 to+125	$^\circ\text{C}$
Storage Temperature	$T_{Stg.}$	-50 to+150	$^\circ\text{C}$
Approximate Weight		6.5	lb
		2.95	Kg
Mounting Force		16,000-20,000	lbs
		71.2 - 89.0	KNewtons

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

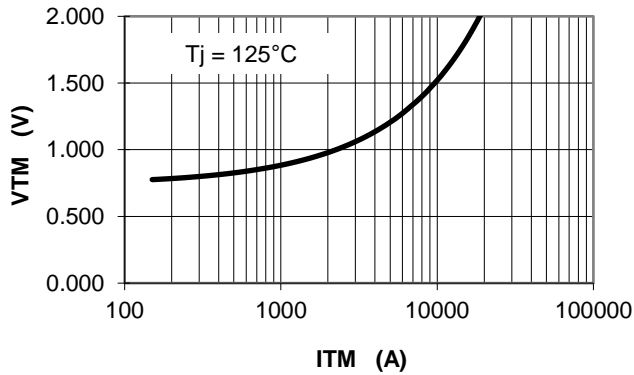
Electrical Characteristics, T_j=25°C unless otherwise specified

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward						
Leakage Current	I _{DRM}	T _j =125°C, V _{DRM} =Rated			300	ma
Repetitive Peak Reverse						
Leakage Current	I _{RRM}	T _j =125°C, V _{RRM} =Rated			300	ma
Peak On-State Voltage	V _{TM}	T _j =125°C, I _{TM} =4000A			1.15	V
V _{TM} Model, Low Level	V ₀	T _j =125°C			0.848	V
V _{TM} = V ₀ + r•I _{TM}	r	15% I _{TM} - π•I _{TM}			6.58E-02	mΩ
V _{TM} Model, High Level	V ₀	T _j =125°C			1.117	V
V _{TM} = V ₀ + r•I _{TM}	r	π•I _{TM} - I _{TSM}			4.74E-02	mΩ
V _{TM} Model, 4-Term	A	T _j =125°C			0.770	
V _{TM} = A + B•Ln(I _{TM}) +	B	15%I _{TM} - I _{TSM}			-0.013	
C•(I _{TM}) + D•(I _{TM}) ^{1/2}	C				3.30E-05	
	D				5.40E-03	
Turn-On Delay Time	t _d	V _D = 0.5•V _{DRM} Gate Drive: 40V - 20Ω		4		us
Turn-Off Time	t _q	T _j =125°C dv/dt = 20V/us to 67% V _{DRM}			500	us
dv/dt _(crit)	dv/dt	T _j =125°C Exp. Waveform V _D =67% Rated	500			V/us
Gate Trigger Current	I _{GT}	T _j =25°C V _D = 12V	30	150	200	ma
Gate Trigger Voltage	V _{GT}		0.8	2.0	4.0	V
Peak Reverse Gate Voltage	V _{GRM}				5	V

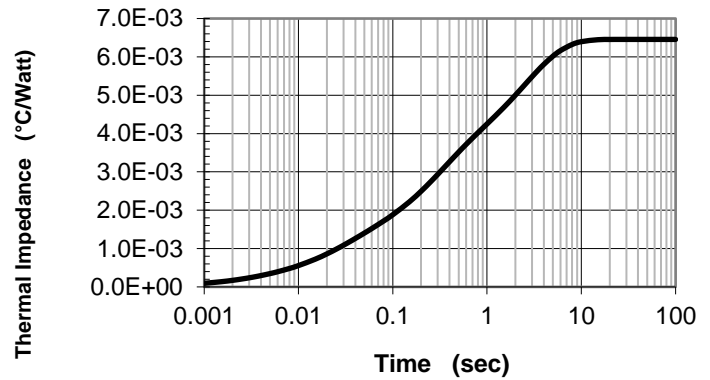
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Rating			
			max			
Thermal Resistance						
Junction to Case	Rθ _{jc}	Double side cooled			0.0065	°C/Watt
Case to Sink	Rθ _{cs}	Double side cooled			0.0015	°C/Watt
Thermal Impedance Model	Zθ _{jc}	Double side cooled				
$Z\theta_{jc}(t) = \Sigma(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$						
where: N = 1 2 3 4						
$A(N) = 1.43E-04 \quad 9.08E-04 \quad 2.18E-03 \quad 3.23E-03$						
$\text{Tau}(N) = 2.62E-03 \quad 2.31E-02 \quad 2.50E-01 \quad 2.50E+00$						

Maximum On-State Voltage Drop

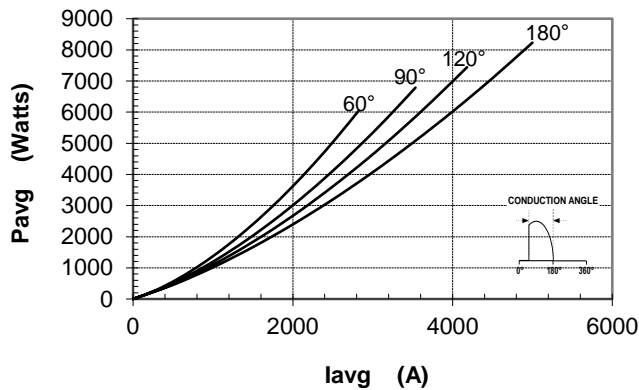


MAXIMUM TRANSIENT THERMAL IMPEDANCE



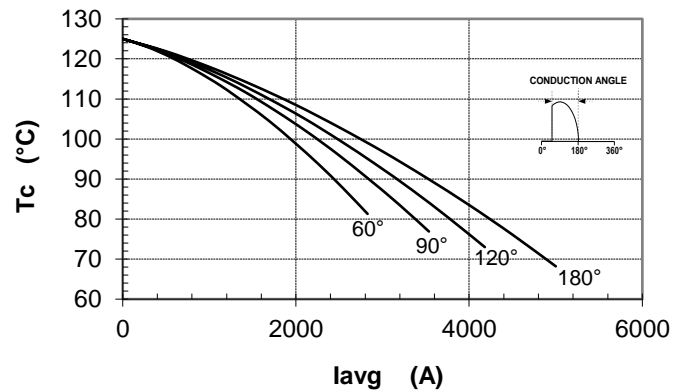
Maximum On-State Power Dissipation

Sinusoidal Waveform



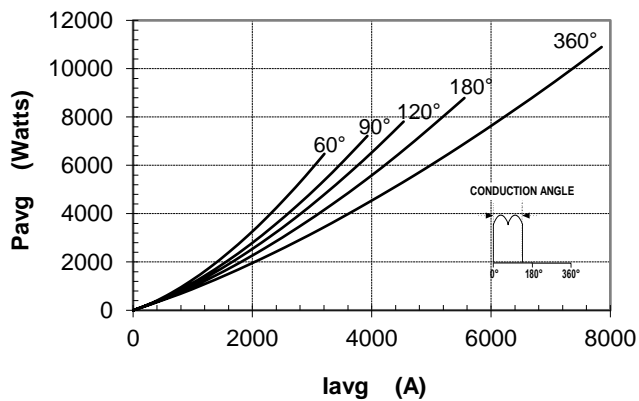
Maximum Allowable Case Temperature

Sinusoidal Waveform



Maximum On-State Power Dissipation

Square Waveform



Maximum Allowable Case Temperature

Square Waveform

