Nihon Inter Electronics Corporation

THYRISTOR MODULE

222A / 800V

P A T 1 0 0 8

P A H 1 0 0 8

FEATURES

* Isolated Base
* Dual Thyristors or Thyristor and Diode Anti-Parallel Circuit
* High Surge Capability
* UL Recognized, File No. E187184

TYPICAL APPLICATIONS

* AC phase control
* AC switch

OUTLINE DRAWING

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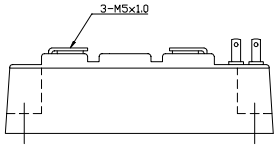
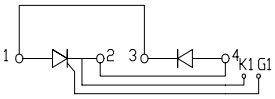




Maximum Ratings

Approx Net Weight:155g

Parameter	Symbol	Grade	Unit
		PAT/PAH1008	
Repetitive Peak Off-State Voltage	V_{DRM}	800	V
Non Repetitive Peak Off-State Voltage	V_{DSM}	960	

Parameter		Conditions	Max Rated Value	Unit
RMS On-State Current	$I_{T(RMS)}$	50Hz Half Sine Wave condition Tc=82℃	222	A
Surge On-State Current	I_{FSM}	50 Hz Half Sine Wave,1Pulse Non-Repetitive	2000	A
I Squared t	I^2t	2msec to 10msec	20000	A^2s
Critical Rate of Turned-On Current	di/dt	V_D=2/3V_{DRM}, I_{TM}=2·I_O, Tj=125℃ I_G=200mA, di_G/dt=0.2A/μs	100	A/μs
Peak Gate Power	P_{GM}		5	W
Average Gate Power	$P_{G(AV)}$		1	W
Peak Gate Current	I_{GM}		2	A
Peak Gate Voltage	V_{GM}		10	V
Peak Gate Reverse Voltage	V_{RGM}		5	V
Operating JunctionTemperature Range	Tjw		-40 to +125	℃
Storage Temperature Range	Tstg		-40 to +125	℃
Isoration Voltage	Viso	Base Plate to Terminals, AC1min	2000	V
Mounting torque — Case mounting	Ftor	M5 Screw	2.4 to 2.8	N•m
Mounting torque — Terminals	Ftor	M5 Screw	2.4 to 2.8	N•m

Value per 1 Arm

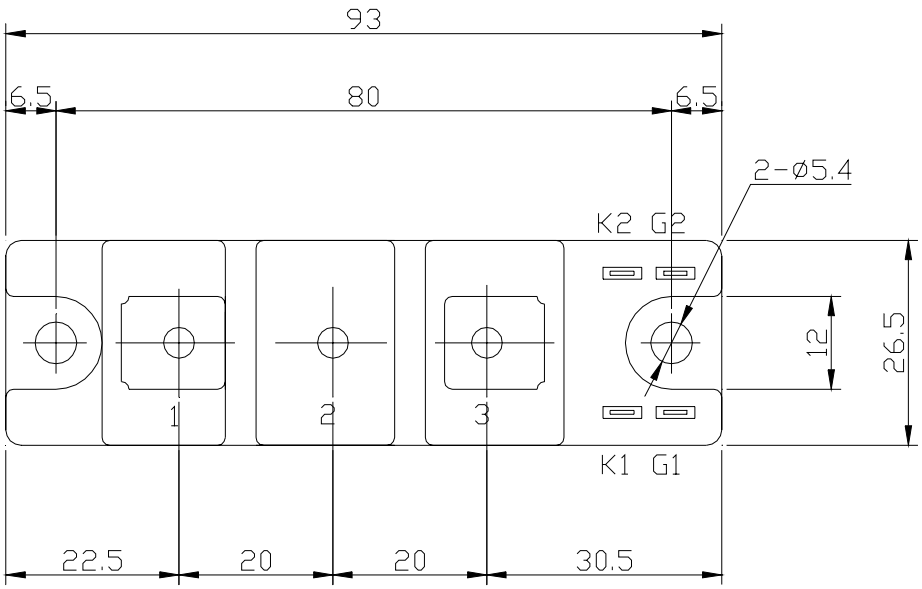
Electrical • Thermal Characteristics

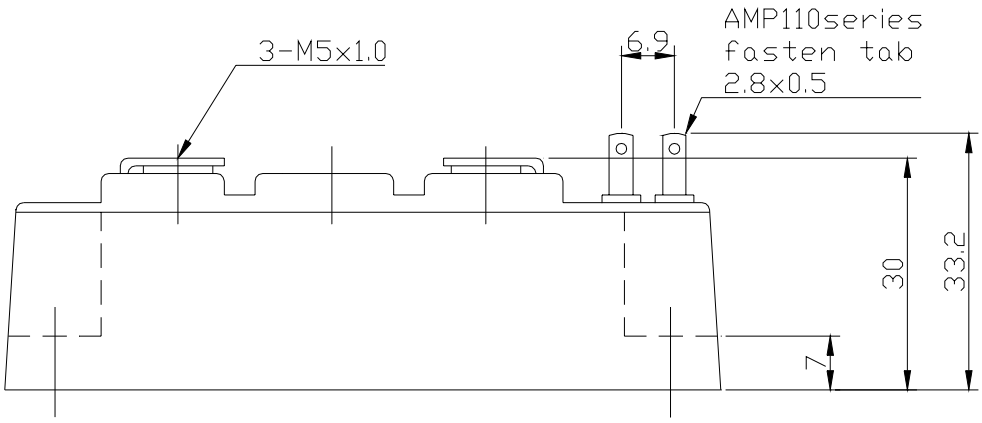
Characteristics	Symbol	Test Conditions		Maximum Value.			Unit
				Min.	Typ.	Max.	
Peak Off-State Current	I_{DM}	V_{DM}= V_{DRM}, Tj=125℃				40	mA
Peak On-State Voltage	V_{TM}	I_{TM}= 300A, Tj=25℃				1.38	V
Gate Current to Trigger	I_{GT}	V_D=6V,I_T=1A	Tj=-40℃			200	mA
			Tj=25℃			100	
			Tj=125℃			50	
Gate Voltage to Trigger	V_{GT}	V_D=6V,I_T=1A	Tj=-40℃			4	V
			Tj=25℃			2.5	
			Tj=125℃			2	
Gate Non-Trigger Voltage	V_{GD}	V_D=2/3V_{DRM} Tj=125℃		0.25			V
Critical Rate of Rise of Off-State Voltage	dv/dt	V_D=2/3V_{DRM} Tj=125℃		500			V/μs
Turn-Off Time	tq	I_{TM}=I_O,V_D=2/3V_{DRM} dv/dt=20V/μs, V_R=100V -di/dt=20A/μs, Tj=125℃			100		μs
Turn-On Time	tgt	Tj=25℃, I_{TM}=$I_{T(RMS)}$ V_D=100V, I_G=200mA di_G/dt=0.2A/μs			6		μs
Delay Time	td				2		μs
Rise Time	tr				4		μs
Latching Current	I_L	Tj=25℃			100		mA
Holding Current	I_H	Tj=25℃			50		
Thermal Resistance *1	Rth(j-c)	Junction to Case				0.15	℃/W
	Rth(c-f)	Base Plate to Heat Sink with Thermal Compound				0.1	

Value Per 1Arm

*1: Value Per Module

PAT/PAH1008 OUTLINE DRAWING (Dimensions in mm)





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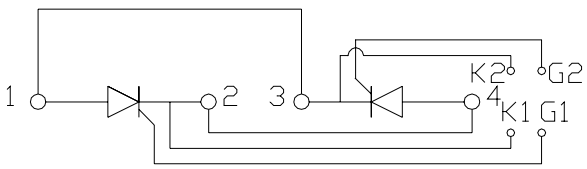

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