ELECTRONICS, INC.
44 FARRAND STREET
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NTE5570, NTE5572, & NTE5574
Silicon Controlled Rectifier
for Phase Control Applications

Electrical Characteristics: (Maximum values @ T_J = +125°C unless otherwise specified)

Repetitive Peak Voltages, V_{DRM} & V_{RRM}
- NTE5570 . . . . . 200V
- NTE5572 . . . . . 600V
- NTE5574 . . . . . 1200V

Non–Repetitive Peak Reverse Blocking Voltage, V_{RSM}
- NTE5570 . . . . . 500V
- NTE5572 . . . . . 900V
- NTE5574 . . . . . 1300V

Average On–State Current (Half Sine Wave, 180°, T_C = +85°C), $I_{T(AV)}$ 80A

RMS On–State Current (DC @ T_C = +75°C), $I_{T(RMS)}$ 125A

Peak One–Cycle, Non–Repetitive Surge Current (10ms Duration, Sinusoidal Half Wave), I_{TSM}
- No Voltage Reapplied 1900A
- 100% V_{RRM} Reapplied 1600A

Maximum I^2t for Fusing (10ms Duration, Sinusoidal Half Wave), I^2t
- No Voltage Reapplied . . . . . 18000A^2sec
- 100% V_{RRM} Reapplied . . . . . 12700A^2sec

Peak Positive Gate Current (5ms Pulse Width), I_{GM} 3A

Peak Positive Gate Voltage (5ms Pulse Width), $+V_{GM}$ 20V

Peak Negative Gate Voltage (5ms Pulse Width), $–V_{GM}$ 10V

Average Gate Power (f = 50Hz, Duty Cycle = 50%), P_G 3W

Peak Gate Power (50ms Pulse Width), P_{GM} 12W

Rate of Rise of Off–State Voltage (Exponential to 67% Rated V_{DRM}), dv/dt 500V/µs

Rate of Rise of ON–State Current, di/dt
(Gate Drive 20V, 65Ω, with t_r = 0.5µs, V_d = Rated V_{DRM}, I_{TM} = 2 x di/dt snubber 0.2µF)
- Non–Repetitive 300A/µs

Typical Delay Time, t_d
(Gate Pulse: 10V, 15Ω Source, t_p = 6µs, t_r = 0.1µs, V_d = rated V_{DRM}, I_{TM} = 50A) 1µs

Typical Turn–On Time, t_q
(I_{TM} = 50A, di/dt = –5A/µs min, V_R = 50V, dv/dt = 20V/µs, Gate Bias: 0V 25Ω, t_p = 500µs) 110µs

On–State Voltage (I_{Pk} = 250A, 10ms Sine Pulse), V_{TM} 1.6V

Repetitive Peak Off–State Current (At V_{DRM}), I_{DRM} 15mA

Repetitive Peak Reverse Current (At V_{RRM}), I_{RRM} 15mA

Maximum Gate Current Required to Trigger, I_{GT}
(6V Anode–to–Cathode Applied, T_J = +25°C) 120mA

Maximum Gate Voltage Required to Trigger, V_{GT}
(6V Anode–to–Cathode Applied, T_J = +25°C) 2.5V

Maximum Holding (Anode Supply 12V Resistive Load, T_J = +25°C), I_H 150mA

Maximum Gate Voltage which will not Trigger any Device, V_{GD} 0.25V

Electrical Characteristics (Cont'd): (Maximum values @ T_J = +125°C unless otherwise specified)

Operating Temperature Range, T_J . . . . . –40° to +125°C

Storage Temperature Range, T_{stg} . . . . . –40° to +150°C

Thermal Resistance, Junction–to–Case (DC Operation), R_{thJC} . . . . . 0.3°C/W

Thermal Resistance, Case–to–Heat Sink, $R_{thC–HS}$

(Mounting Surface Smooth, Flat, and Greased) . . . . . 0.1°C/W