MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MPM3002

Advance Information

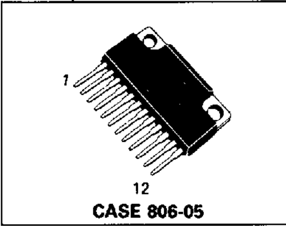
TMOS ICePAK Power Module

P-Channel Power MOSFET and N-Channel SENSEFET™ Product in a Full H-Bridge Configuration

TMOS POWER MOSFET
H-BRIDGE
100 VOLTS
8 AMPERES

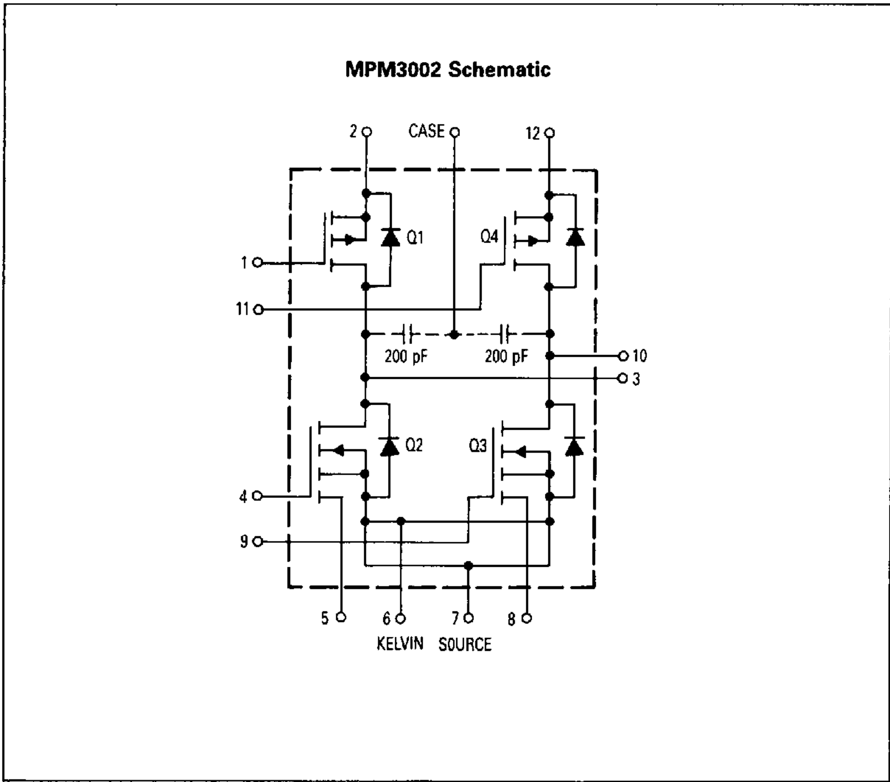
The MPM3002 is a H-Bridge power circuit with lossless current sensing capability. The upper legs of the bridge consists of P-Channel power MOSFETs and the lower legs of the bridge consist of two SENSEFET devices. This power circuit packaged in the ICePAK package is ideal for applications such as servo motor drives, stepper motor controls and switching power supplies. Features of this product include:

- P and N-Channel Power MOSFET Configuration for Ease of Drive
- Lossless Current Sensing in Each Lower Leg of the H-Bridge
- Isolated Package with 2 kV Isolation Voltage Rating
- High Power Handling Capability — 62.5 Watts
- High Peak Current Handling Capability — 25 Amperes



CASE 806-05

MPM3002 Schematic



This document contains information on a new product. Specifications and information herein are subject to change without notice

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage	(All Types)	V_{DSS}	100	Volts
Drain-to-Gate Voltage (R_{GS} = 1MΩ)	(All Types)	V_{DGR}	100	
Gate-to-Source Voltage	(All Types)	V_{GS}	±20	
Drain-to-Mirror Voltage	(Q2 and Q3)	V_{DM}	100	
Gate-to-Mirror Voltage	(Q2 and Q3)	V_{GM}	±20	
Drain Current — Continuous — Pulsed	(Q2 and Q3)	I_D I_{DM}	12 30	Amps
— Continuous — Pulsed	(Q1 and Q4)	I_D I_{DM}	8 25	
— Continuous — Pulsed	(N/P-Channel Combination)	I_D I_{DM}	8 25	
Sense Current — Continuous — Pulsed	(Q2 and Q3)	I_M I_{MM}	13 33	mA
RMS Isolation Voltage	(Any Pin to Case)	V_{ISO}	2000	Volts
Operating and Storage Temperature Range		T_J, T_{stg}	−40 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Power Dissipation — T_C = 25°C (Any single device) (Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")	P_D	 62 5 62 5 31.25	Watts
Power Derating — Derate above T_C = 25°C (Any single device) (Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")	$1/R_{\theta JC}$	 0.5 0.5 0.25	W/°C
Thermal Resistance — Junction to Case — Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2 35	°C/W
Thermal Coupling Coefficient (Q1 to Q2 or Q4 to Q3) See Table 1 (Q1 to Q3, Q1 to Q4, Q2 to Q3 or Q2 to Q4)	α β	0.5 0 01	—
Maximum Lead Temperature for Soldering Purposes 1/8" from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{MS} = 0 unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	(All Devices)	$V_{(BR)DSS}$	100	—	—	Vdc
Drain-to-Mirror Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	(Q2 and Q3)	$V_{(BR)DMS}$	100	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 80 V, V_{GS} = 0) (V_{DS} = 80 V, V_{GS} = 0, T_J = 125°C)	(Any Single Device)	I_{DSS}	 — —	 — —	 0.2 1	mAdc
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	(Any Single Device)	I_{GSSF}	—	—	100	nAdc
Gate Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	(Any Single Device)	I_{GSSR}	—	—	100	—
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mAdc) (T_J = 125°C)	(Any Single Device)	$V_{GS(th)}$	 2 1	 3 —	 4.5 3.5	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	(Q2 and Q3)	$R_{DS(on)}$	—	—	0.15	Ohms

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C, V_{MS} = 0 unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	(Q1 and Q4)	$R_{DS(on)}$	—	—	0.4	Ohms
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	(Q2 and Q3)	g_{FS}	3	—	—	Mhos
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	(Q1 and Q4)	g_{FS}	2	—	—	Mhos
CURRENT SENSING CHARACTERISTICS (N-Channel, Q2 and Q3)						
Current Mirror Ratio (Cell Ratio) (R_{SENSE} = 0, I_D = 8 A, V_{GS} = 10 V)		n	750	—	850	—
Mirror Compliance Ratio (V_{GS} = 10 Vdc, I_D = 4 Adc)		K_{mc}	—	0.78	—	—
Source Active Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc, R_S = 10 megohm)		$r_{a(on)}$	—	140	—	mΩ
Mirror Active Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{m(on)}$	—	112	—	Ohms
DYNAMIC CHARACTERISTICS (All Types)						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	—	—	900	pF
Output Capacitance		C_{oss}	—	—	450	
Transfer Capacitance		C_{rss}	—	—	200	
SWITCHING CHARACTERISTICS* (N-Channel, Q2 and Q3)						
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 4 A R_{gen} = 50 Ohms)	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	—	120	
Fall Time		t_f	—	—	125	
Total Gate Charge	(V_{DS} = 80 V, I_D = 8 A V_{GS} = 10 V)	Q_g	—	38	45	nC
Gate-Source Charge		Q_{gs}	—	15	—	
Gate-Drain Charge		Q_{gd}	—	23	—	
SWITCHING CHARACTERISTICS* (P-Channel, Q1 and Q4)						
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 4 A R_{gen} = 50 Ohms)	$t_{d(on)}$	—	—	25	ns
Rise Time		t_r	—	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40	
Fall Time		t_f	—	—	60	
Total Gate Charge	(V_{DS} = 80 V, I_D = 8 A V_{GS} = 10 V)	Q_g	—	23	30	nC
Gate-Source Charge		Q_{gs}	—	10	—	
Gate-Drain Charge		Q_{gd}	—	13	—	
SOURCE-DRAIN DIODE CHARACTERISTICS (N-Channel, Q2 and Q3)						
Forward On-Voltage	(I_S = 8 A)	V_{SD}	—	1 2	—	Vdc
Forward Turn-On Time		t_{on}	—	25	—	ns
Reverse Recovery Time		t_{rr}	—	155	—	
SOURCE-DRAIN DIODE CHARACTERISTICS (P-Channel, Q1 and Q4)						
Forward On-Voltage	(I_S = 8 A)	V_{SD}	—	4	—	Vdc
Forward Turn-On Time		t_{on}	—	25	—	ns
Reverse Recovery Time		t_{rr}	—	150	—	

*Indicates Pulse Test: Pulse Width = 300 μs Max, Duty Cycle = 2%
Note 1: Handling precautions to protect against electrostatic discharge is mandatory
Note 2: Do not use the mirror FET independent of the power FET
Note 3: It is recommended that the mirror terminal (M) be shorted to the source terminal (S) when current sensing is not required.