

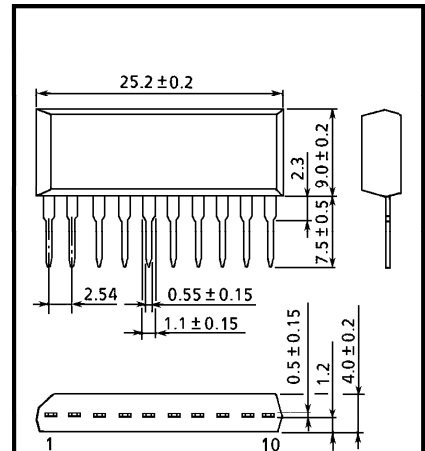
TOSHIBA POWER MOS FET MODULE SILICON P CHANNEL MOS TYPE (L²-π-MOSV 4 IN 1)

MP4211

HIGH POWER, HIGH SPEED SWITCHING APPLICATIONS
 FOR PRINTER HEAD PIN DRIVER AND PULSE MOTOR DRIVER
 FOR SOLENOID DRIVER

INDUSTRIAL APPLICATIONS
 Unit in mm

- 4 V Gate Drive Available
- Small Package by Full Molding (SIP 10 Pin)
- High Drain Power Dissipation (4 Devices Operation)
 : P_T = 4 W (T_a = 25°C)
- Low Drain-Source ON Resistance : R_{DS(ON)} = 0.16 Ω (typ.)
- High Forward Transfer Admittance : |Y_{fs}| = 4.0 S (typ.)
- Low Leakage Current : I_{GSS} = ±10 μA (max.) (V_{GS} = ±16 V)
 I_{DSS} = -100 μA (max.) (V_{DS} = -60 V)
- Enhancement-Mode : V_{th} = -0.8 ~ -2.0 V
 (V_{DS} = -10 V, I_D = -1 mA)

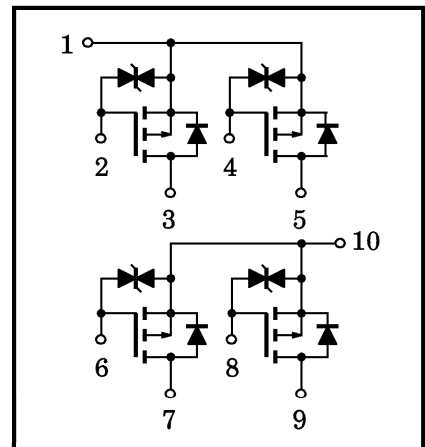


1, 10 SOURCE
 2, 4, 6, 8 GATE
 3, 5, 7, 9 DRAIN
 (PIN 1 AND PIN 10 IS DISCONNECTED INTERNALLY)

JEDEC	—
EIAJ	—
TOSHIBA	2-25A1C

Weight : 2.1 g (typ.)

ARRAY CONFIGURATION



MAXIMUM RATINGS (T_a = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V _{DSS}	-60	V
Drain-Gate Voltage (R _{GS} = 20 kΩ)		V _{DGR}	-60	V
Gate-Source Voltage		V _{GSS}	±20	V
Drain Current	DC	I _D	-5	A
	Pulse	I _{DP}	-20	
Drain Power Dissipation (1 Device Operation, T _a = 25°C)		P _D	2.0	W
Drain Power Dissipation (4 Devices Operation, T _a = 25°C)		P _{DT}	4.0	W
Single Pulse Avalanche Energy*		E _{AS}	273	mJ
Avalanche Current		I _{AR}	-5	A
Repetitive Avalanche Energy**	1 Device Operation	E _{AR}	0.2	mJ
	4 Devices Operation	E _{ART}	0.4	
Channel Temperature		T _{ch}	150	°C
Storage Temperature Range		T _{stg}	-55 ~ 150	°C

Note ;

* Avalanche energy (single pulse) applied condition

V_{DD} = -25 V, Starting T_{ch} = 25°C, L = 14.84 mH, R_G = 25 Ω, I_{AR} = -5 A

** Repetitive rating ; Pulse Width Limited by maximum channel temperature.

This transistor is an electrostatic sensitive device. Please handle with caution.

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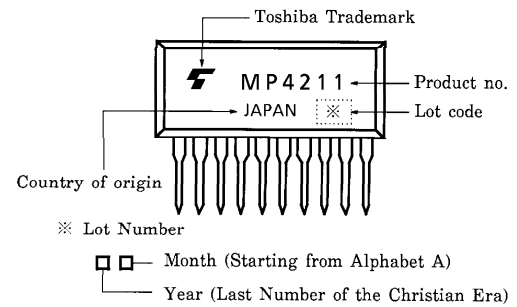
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THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX.	UNIT
Thermal Resistance of Channel to Ambient (4 Devices Operation, Ta = 25°C)	$\Sigma R_{th(ch-a)}$	31.2	°C / W
Maximum Lead Temperature for Soldering Purposes (3.2 mm from Case for t = 10 s)	T _L	260	°C

MARKING



ELECTRICAL CHARACTERISTICS (Ta = 25°C)

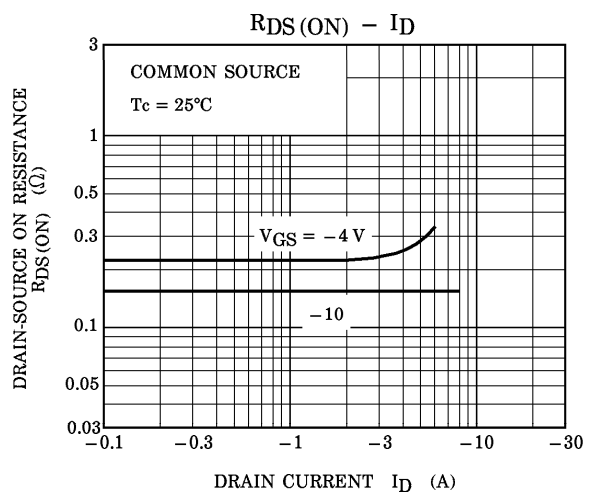
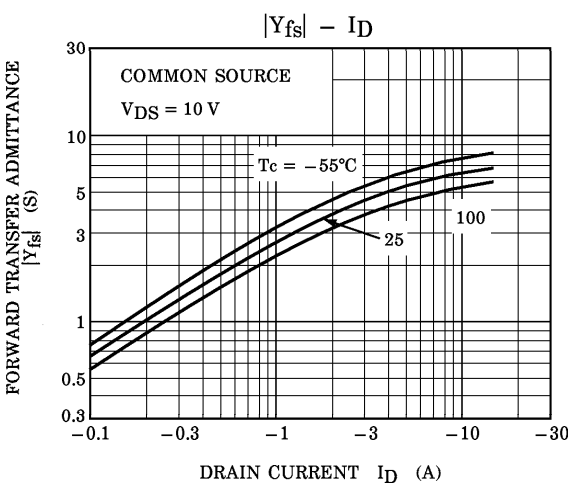
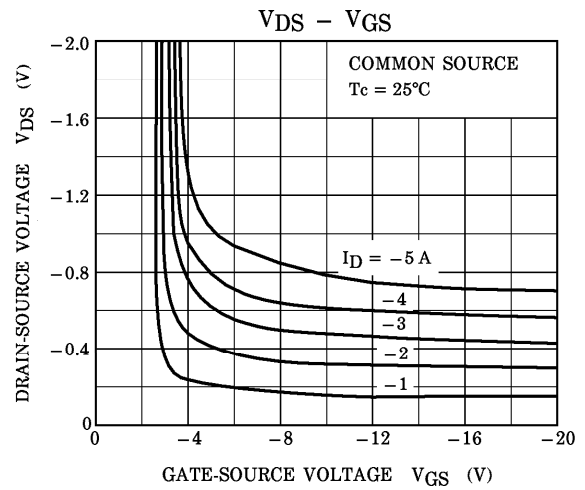
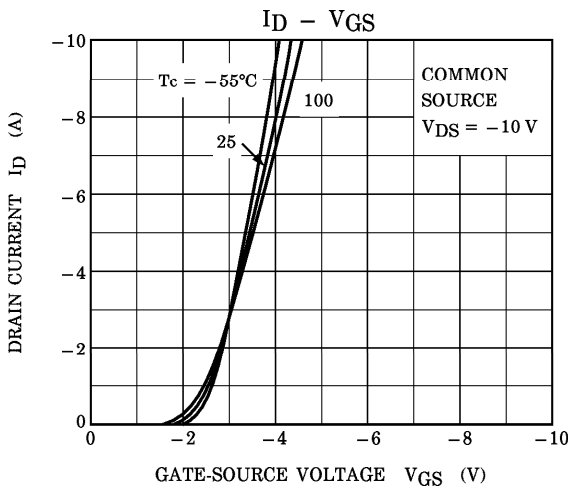
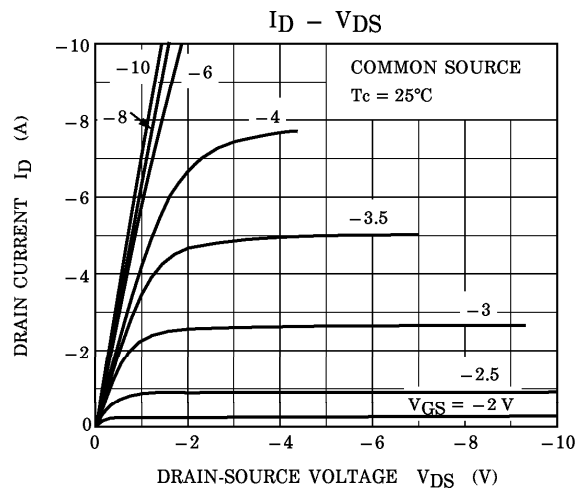
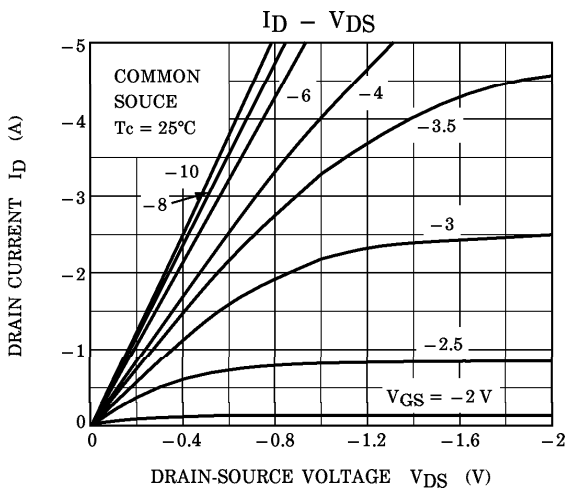
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Gate Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V	—	—	±10	μA	
Drain Cut-off Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V	—	—	-100	μA	
Drain-Source Breakdown Voltage	V(BR) DSS	I _D = -10 mA, V _{GS} = 0 V	-60	—	—	V	
Gate Threshold Voltage	V _{th}	V _{DS} = -10 V, I _D = -1 mA	-0.8	—	-2.0	V	
Drain-Source ON Resistance	R _{DSON}	V _{GS} = -4 V, I _D = -2.5 A	—	0.24	0.28	Ω	
		V _{GS} = -10 V, I _D = -2.5 A	—	0.16	0.19		
Forward Transfer Admittance	Y _{fs}	V _{DS} = -10 V, I _D = -2.5 A	2.0	4.0	—	S	
Input Capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	—	630	—	pF	
Reverse Transfer Capacitance	C _{rss}		—	95	—		
Output Capacitance	C _{oss}		—	290	—		
Switching Time	Rise Time	t _r		—	25	—	ns
	Turn-on Time	t _{on}		—	45	—	
	Fall Time	t _f		—	55	—	
	Turn-off Time	t _{off}		—	200	—	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q _g	V _{DD} = -48 V, V _{GS} = -10 V, I _D = -5 A	—	22	—	nC	
Gate-Source Charge	Q _{gs}	—	—	16	—		
Gate-Drain ("Miller") Charge	Q _{gd}	—	—	6	—		

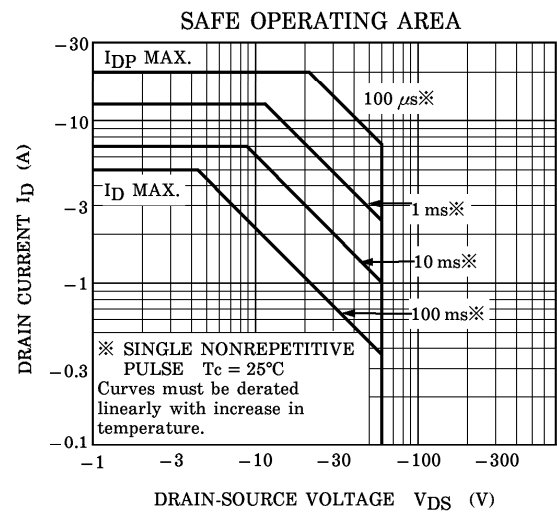
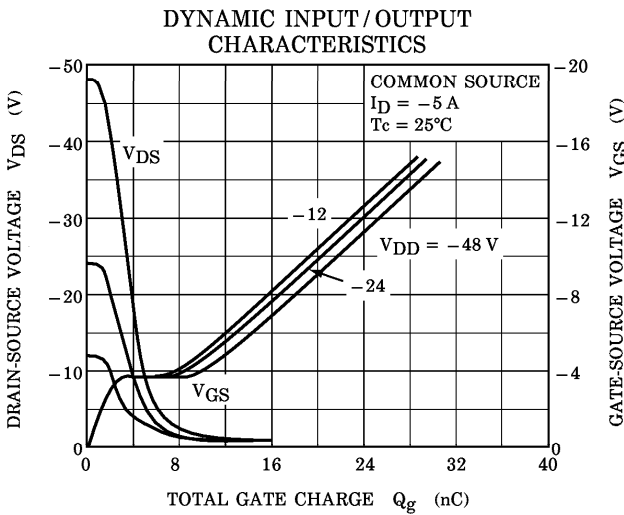
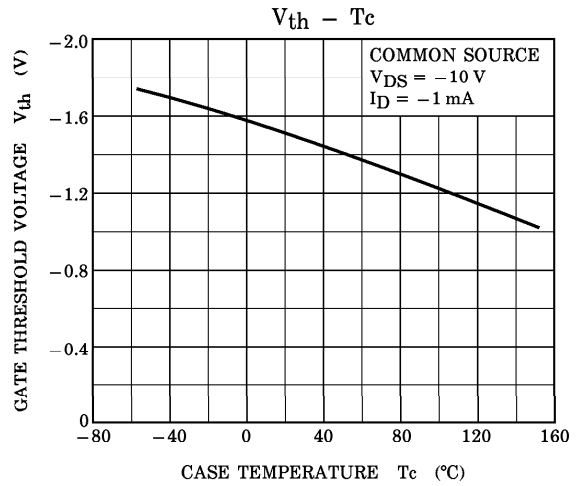
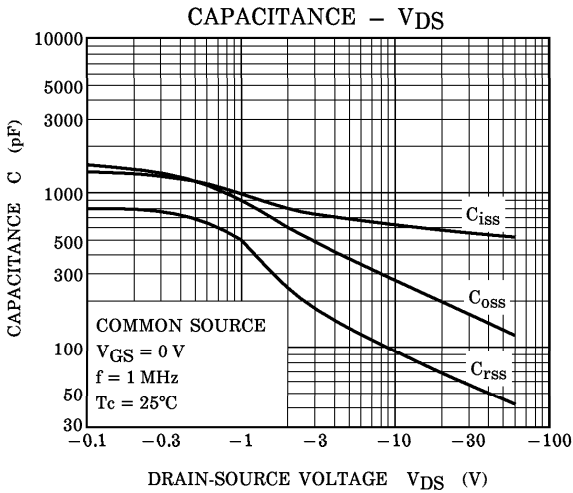
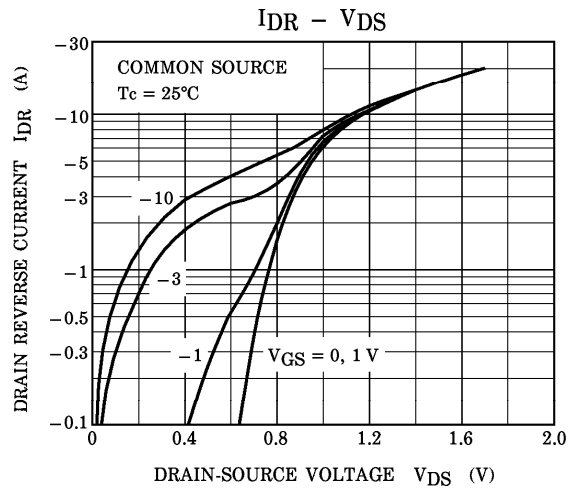
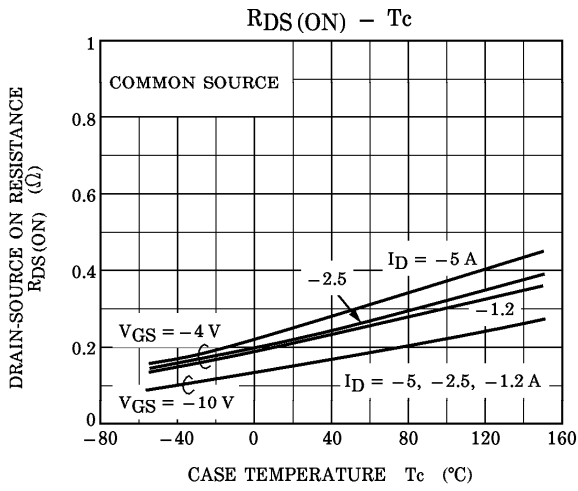
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (Ta = 25°C)

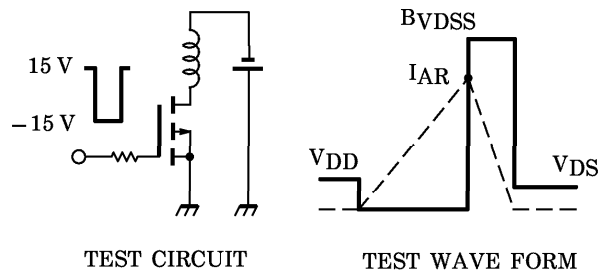
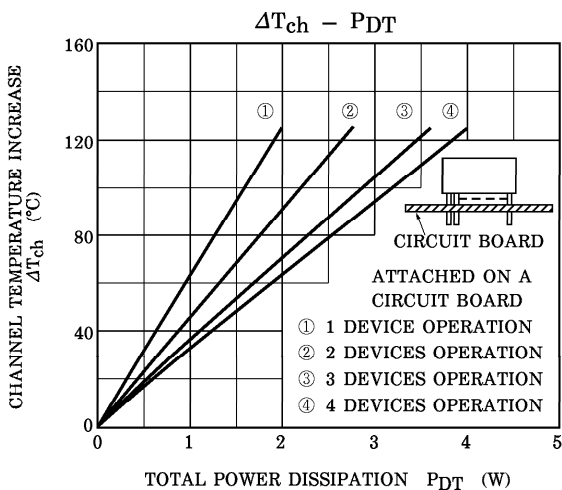
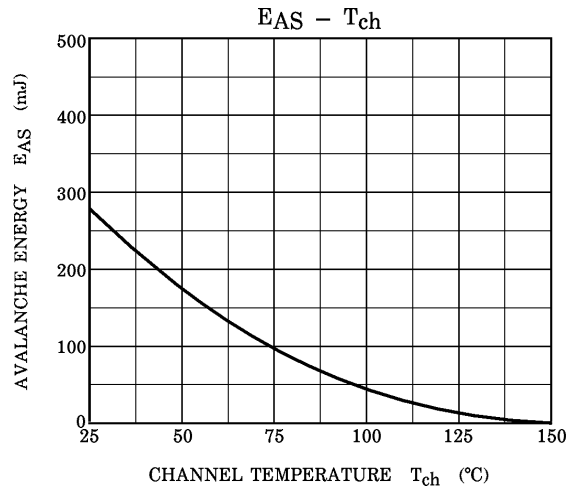
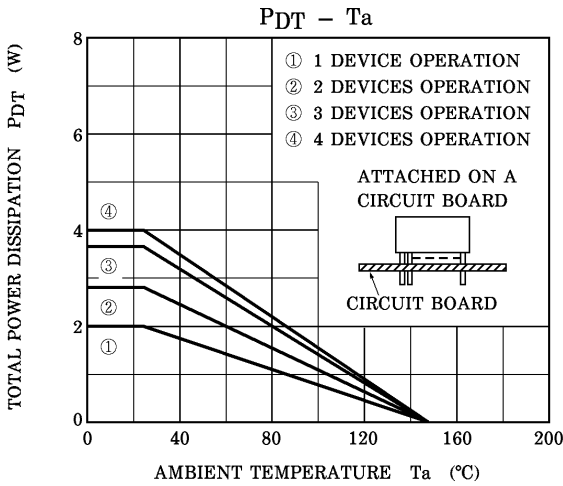
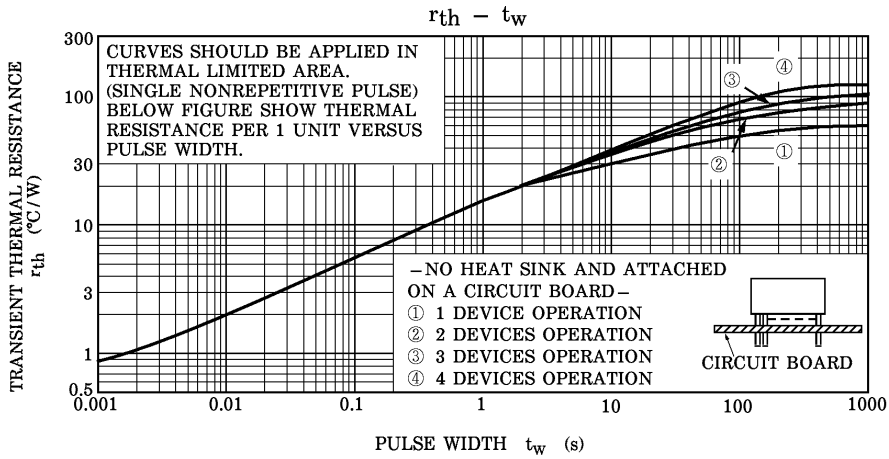
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Continuous Drain Reverse Current	I _{DR}	—	—	—	-5	A
Pulse Drain Reverse Current	I _{DRP}	—	—	—	-20	A
Diode Forward Voltage	V _{DSF}	I _{DR} = -5 A, V _{GS} = 0 V	—	—	1.7	V
Reverse Recovery Time	t _{rr}	I _{DR} = -5 A, V _{GS} = 0 V	—	80	—	ns
Reverse Recovery Charge	Q _{rr}	dI _{DR} / dt = 50 A / μs	—	0.1	—	μC

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Peak $I_{AR} = -5$ A, $R_G = 25 \Omega$, $V_{DD} = -25$ V, $L = 14.84$ mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$