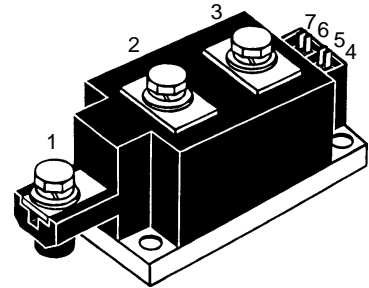


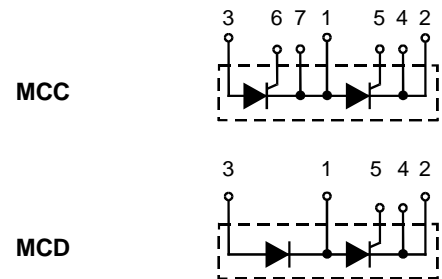
Thyristor Modules Thyristor/Diode Modules

$I_{TRMS} = 2x 520 A$
 $I_{TAVM} = 2x 320 A$
 $V_{RRM} = 1200-1800 V$

V_{RSM}	V_{RRM}	Type	
V_{DSM}	V_{DRM}		
V	V		
1300	1200	MCC 312-12io1	MCD 312-12io1
1500	1400	MCC 312-14io1	MCD 312-14io1
1700	1600	MCC 312-16io1	MCD 312-16io1
1900	1800	MCC 312-18io1	MCD 312-18io1



Symbol	Test Conditions	Maximum Ratings	
I_{TRMS}, I_{FRMS} I_{TAVM}, I_{FAVM}	$T_{VJ} = T_{VJM}$ $T_C = 85^\circ C; 180^\circ$ sine	520	A
		320	A
I_{TSM}, I_{FSM}	$T_{VJ} = 45^\circ C;$ $V_R = 0$	$t = 10$ ms (50 Hz)	A
		$t = 8.3$ ms (60 Hz)	A
	$T_{VJ} = T_{VJM}$ $V_R = 0$	$t = 10$ ms (50 Hz)	A
		$t = 8.3$ ms (60 Hz)	A
$\int i^2 dt$	$T_{VJ} = 45^\circ C$ $V_R = 0$	$t = 10$ ms (50 Hz)	A^2s
		$t = 8.3$ ms (60 Hz)	A^2s
	$T_{VJ} = T_{VJM}$ $V_R = 0$	$t = 10$ ms (50 Hz)	A^2s
		$t = 8.3$ ms (60 Hz)	A^2s
$(di/dt)_{cr}$	$T_{VJ} = T_{VJM}$ $f = 50$ Hz, $t_p = 200$ μs $V_D = 2/3 V_{DRM}$ $I_G = 1$ A, $di_G/dt = 1$ A/ μs	repetitive, $I_T = 960$ A	100 $A/\mu s$
		non repetitive, $I_T = I_{TAVM}$	500 $A/\mu s$
$(dv/dt)_{cr}$	$T_{VJ} = T_{VJM}; V_{DR} = 2/3 V_{DRM}$ $R_{GK} = \infty;$ method 1 (linear voltage rise)		1000 $V/\mu s$
P_{GM}	$T_{VJ} = T_{VJM}$ $I_T = I_{TAVM}$	$t_p = 30$ μs	120 60 20 10 W W W V
P_{GAV}		$t_p = 500$ μs	
V_{RGM}			
T_{VJ}			-40...+140 140 -40...+125 $^\circ C$ $^\circ C$ $^\circ C$
T_{VJM}			
T_{stg}			
V_{ISOL}	50/60 Hz, RMS	$t = 1$ min	3000 3600 V~ V~
		$I_{ISOL} \leq 1$ mA	
M_d	Mounting torque (M6)		4.5-7/40-62 Nm/lb.in.
	Terminal connection torque (M8)		11-13/97-115 Nm/lb.in.
Weight	Typical including screws		750 g



Features

- International standard package
- Direct copper bonded Al_2O_3 -ceramic with copper base plate
- Planar passivated chips
- Isolation voltage 3600 V~
- UL registered E 72873
- Keyed gate/cathode twin pins

Applications

- Motor control, softstarter
- Power converter
- Heat and temperature control for industrial furnaces and chemical processes
- Lighting control
- Solid state switches

Advantages

- Simple mounting
- Improved temperature and power cycling
- Reduced protection circuits

Data according to IEC 60747 and refer to a single thyristor/diode unless otherwise stated. IXYS reserves the right to change limits, test conditions and dimensions

Symbol	Test Conditions	Characteristic Values
I_{RRM}, I_{DRM}	$T_{VJ} = T_{VJM}; V_R = V_{RRM}; V_D = V_{DRM}$	40 mA
V_T, V_F	$I_T, I_F = 600 \text{ A}; T_{VJ} = 25^\circ\text{C}$	1.32 V
V_{T0}	For power-loss calculations only ($T_{VJ} = 140^\circ\text{C}$)	0.8 V
r_T		0.68 mΩ
V_{GT}	$V_D = 6 \text{ V}; T_{VJ} = 25^\circ\text{C}$	2 V
	$T_{VJ} = -40^\circ\text{C}$	3 V
I_{GT}	$V_D = 6 \text{ V}; T_{VJ} = 25^\circ\text{C}$	150 mA
	$T_{VJ} = -40^\circ\text{C}$	220 mA
V_{GD}	$T_{VJ} = T_{VJM}; V_D = 2/3 V_{DRM}$	0.25 V
I_{GD}	$T_{VJ} = T_{VJM}; V_D = 2/3 V_{DRM}$	10 mA
I_L	$T_{VJ} = 25^\circ\text{C}; t_p = 30 \mu\text{s}; V_D = 6 \text{ V}$ $I_G = 0.45 \text{ A}; di_G/dt = 0.45 \text{ A}/\mu\text{s}$	200 mA
I_H	$T_{VJ} = 25^\circ\text{C}; V_D = 6 \text{ V}; R_{GK} = \infty$	150 mA
t_{gd}	$T_{VJ} = 25^\circ\text{C}; V_D = 1/2 V_{DRM}$ $I_G = 1 \text{ A}; di_G/dt = 1 \text{ A}/\mu\text{s}$	2 μs
t_q	$T_{VJ} = T_{VJM}; I_T = 300 \text{ A}, t_p = 200 \mu\text{s}; -di/dt = 10 \text{ A}/\mu\text{s}$ typ. $V_R = 100 \text{ V}; dv/dt = 50 \text{ V}/\mu\text{s}; V_D = 2/3 V_{DRM}$	200 μs
Q_S	$T_{VJ} = 125^\circ\text{C}; I_T, I_F = 300 \text{ A}; -di/dt = 50 \text{ A}/\mu\text{s}$	760 μC
I_{RM}		275 A
R_{thJC}	per thyristor (diode); DC current per module	0.12 K/W
R_{thJK}	per thyristor (diode); DC current per module	0.06 K/W
	other values see Fig. 8/9	0.16 K/W
		0.08 K/W
d_s	Creeping distance on surface	12.7 mm
d_A	Creepage distance in air	9.6 mm
a	Maximum allowable acceleration	50 m/s ²

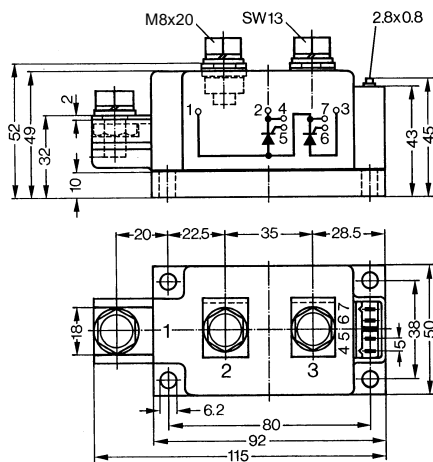
Optional accessories for modules

Keyed Gate/Cathode twin plugs with wire length = 350 mm, gate = yellow, cathode = red

Type ZY 180 L (L = Left for pin pair 4/5) } UL 758, style 1385,
Type ZY 180 R (R = Right for pin pair 6/7) } CSA class 5851, guide 460-1-1

Dimensions in mm (1 mm = 0.0394")

MCC



MCD

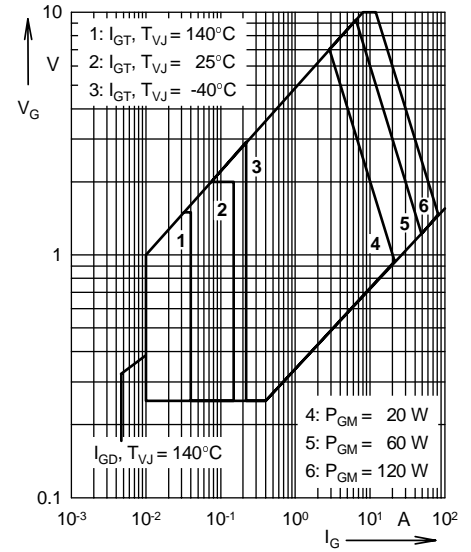
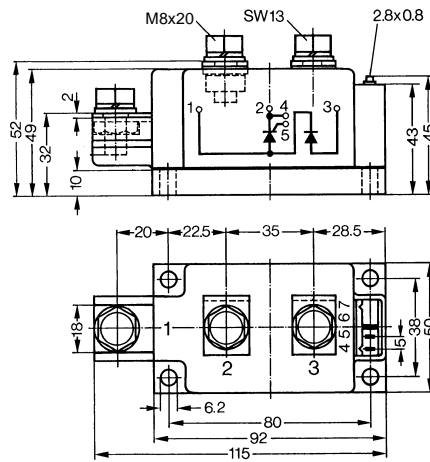


Fig. 1 Gate trigger characteristics

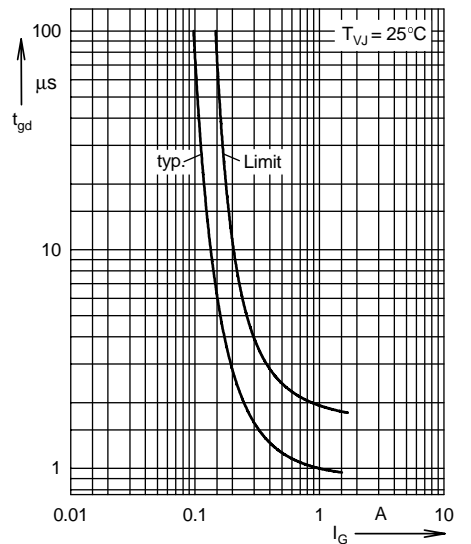


Fig. 2 Gate trigger delay time