

IR2130/IR2132(J)(S) & (PbF)

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
 Fully operational to +600V
 Tolerant to negative transient voltage
 dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- Cross-conduction prevention logic
- Also available LEAD-FREE

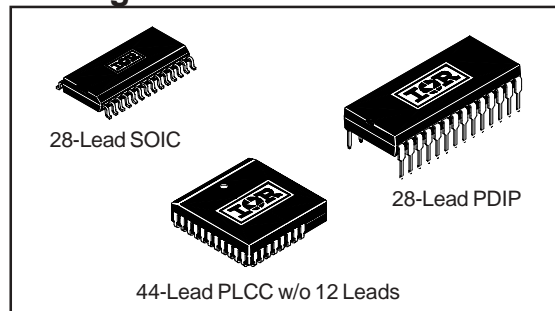
Description

The IR2130/IR2132(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain $\overline{\text{FAULT}}$ signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

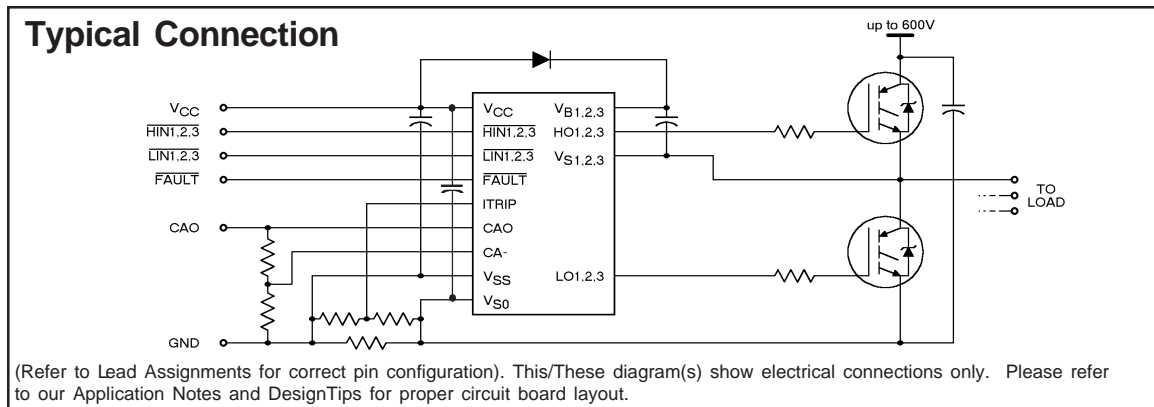
Product Summary

V_{OFFSET}	600V max.
$I_{\text{O}+/-}$	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{\text{on/off}}$ (typ.)	675 & 425 ns
Deadtime (typ.)	2.5 μs (IR2130) 0.8 μs (IR2132)

Packages



Typical Connection



IR2130/IR2132(J)(S) & (PbF)

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{S0} . The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 50 through 53.

Symbol	Definition	Min.	Max.	Units	
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	625	V	
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$		
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3} - 0.3$	$V_{B1,2,3} + 0.3$		
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25		
V_{SS}	Logic Ground	$V_{CC} - 25$	$V_{CC} + 0.3$		
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$		
V_{IN}	Logic Input Voltage (HIN1,2,3, LIN1,2,3 & ITRIP)	$V_{SS} - 0.3$	($V_{SS} + 15$) or ($V_{CC} + 0.3$) whichever is lower		
V_{FLT}	FAULT Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
V_{CAO}	Operational Amplifier Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
V_{CA-}	Operational Amplifier Inverting Input Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50		V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$				W
	(28 Lead DIP)	—	1.5		
	(28 Lead SOIC)	—	1.6		
	(44 Lead PLCC)	—	2.0	$^\circ\text{C/W}$	
R_{thJA}	Thermal Resistance, Junction to Ambient				
	(28 Lead DIP)	—	83		
	(28 Lead SOIC)	—	78	$^\circ\text{C}$	
	(44 Lead PLCC)	—	63		
T_J	Junction Temperature	—	150	$^\circ\text{C}$	
T_S	Storage Temperature	-55	150		
T_L	Lead Temperature (Soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0} . The V_S offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figure 54.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3} + 10$	$V_{S1,2,3} + 20$	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage (HIN1,2,3, LIN1,2,3 & ITRIP)	V_{SS}	$V_{SS} + 5$	
V_{FLT}	FAULT Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	$V_{SS} + 5$	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS}	$V_{SS} + 5$	
T_A	Ambient Temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of ($V_{S0} - 5V$) to ($V_{S0} + 600V$). Logic state held for V_S of ($V_{S0} - 5V$) to ($V_{S0} - V_{BS}$). (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins, CA- and CAO pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} , C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 3 through 5.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	11	500	675	850	ns	
t_{off}	Turn-Off Propagation Delay	12	300	425	550		$V_{IN} = 0$ & 5V
t_r	Turn-On Rise Time	13	—	80	125		$V_{S1,2,3} = 0$ to 600V
t_f	Turn-Off Fall Time	14	—	35	55		
t_{itrip}	ITRIP to Output Shutdown Prop. Delay	15	400	660	920		V_{IN} , $V_{ITRIP} = 0$ & 5V
t_{bl}	ITRIP Blanking Time	—	—	400	—		$V_{ITRIP} = 1V$
t_{flt}	ITRIP to \overline{FAULT} Indication Delay	16	335	590	845		V_{IN} , $V_{ITRIP} = 0$ & 5V
$t_{flt.in}$	Input Filter Time (All Six Inputs)	—	—	310	—		$V_{IN} = 0$ & 5V
t_{fltclr}	LIN1,2,3 to \overline{FAULT} Clear Time	17	6.0	9.0	12.0		V_{IN} , $V_{ITRIP} = 0$ & 5V
DT	Deadtime (IR2130)	18	1.3	2.5	3.7		μs
	(IR2132)	18	0.4	0.8	1.2		
SR+	Operational Amplifier Slew Rate (+)	19	4.4	6.2	—	V/ μs	
SR-	Operational Amplifier Slew Rate (-)	20	2.4	3.2	—		

NOTE: For high side PWM, HIN pulse width must be $\geq 1.5\mu s$

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	21	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	22	—	—	0.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	23	400	490	580	mV	
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	24	—	—	100		$V_{IN} = 0V$, $I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	25	—	—	100	$V_{IN} = 5V$, $I_O = 0A$	
I_{LK}	Offset Supply Leakage Current	26	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} Supply Current	27	—	15	30		$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	28	—	3.0	4.0	mA	$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	29	—	450	650		$V_{IN} = 0V$
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	30	—	225	400	μA	$V_{IN} = 5V$
I_{ITRIP+}	"High" ITRIP Bias Current	31	—	75	150		ITRIP = 5V
I_{ITRIP-}	"Low" ITRIP Bias Current	32	—	—	100	nA	ITRIP = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	33	7.5	8.35	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	34	7.1	7.95	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	35	8.3	9.0	9.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	36	8.0	8.7	9.4		
$R_{on,FLT}$	\overline{FAULT} Low On-Resistance	37	—	55	75		Ω

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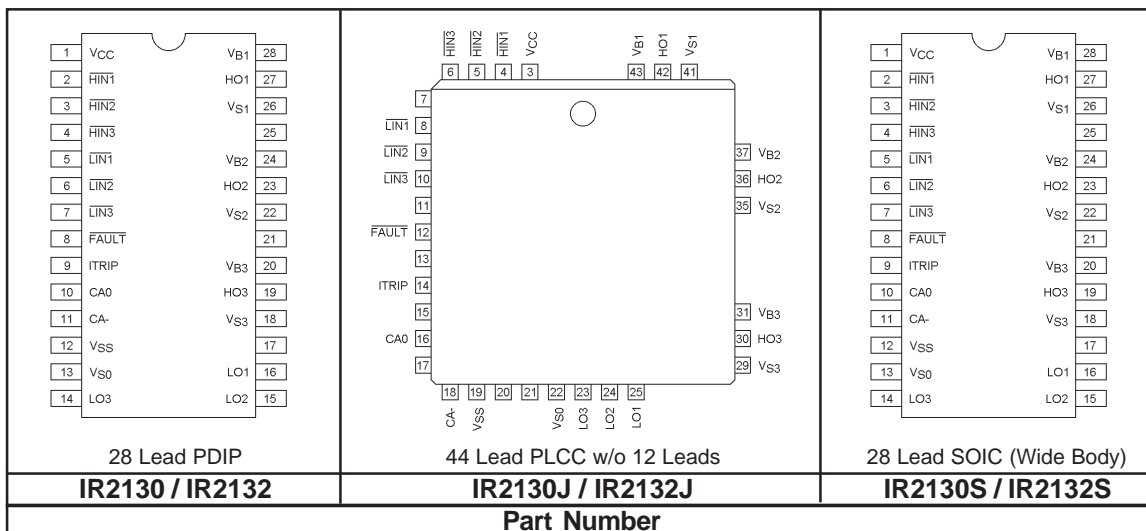
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Static Electrical Characteristics -- Continued

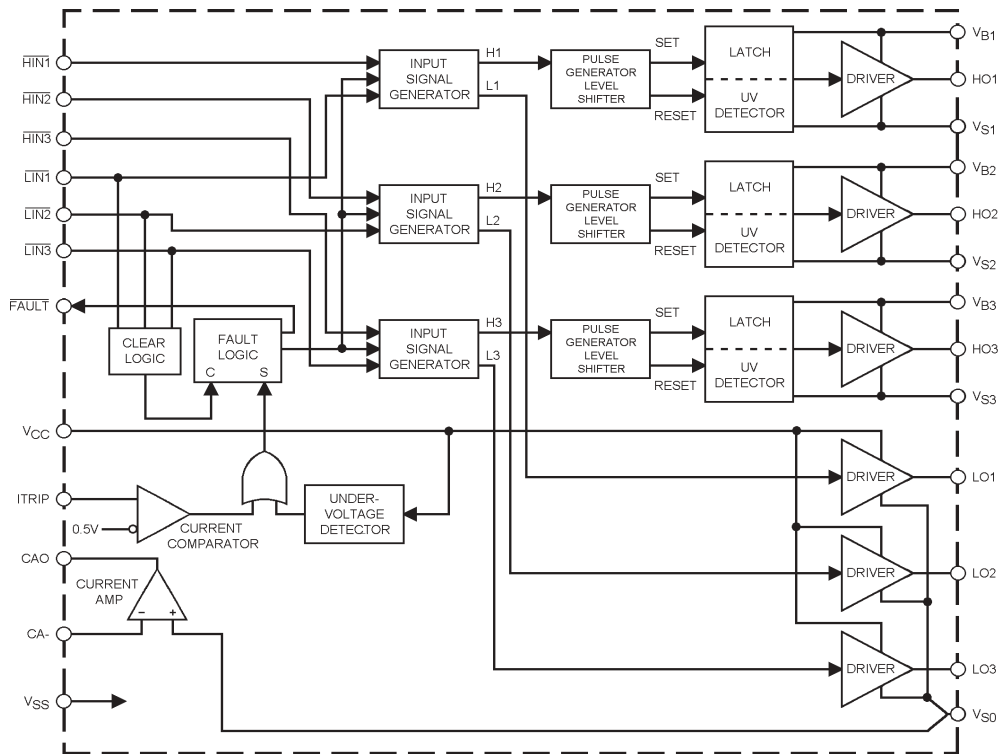
V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $HIN1,2,3$ & $LIN1,2,3$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: $HO1,2,3$ or $LO1,2,3$.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
I_{O+}	Output High Short Circuit Pulsed Current	38	200	250	—	mA	$V_O = 0V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	39	420	500	—		$V_O = 15V$, $V_{IN} = 5V$ $PW \leq 10 \mu s$
V_{OS}	Operational Amplifier Input Offset Voltage	40	—	—	30	mV	$V_{S0} = V_{CA-} = 0.2V$
I_{CA-}	CA- Input Bias Current	41	—	—	4.0	nA	$V_{CA-} = 2.5V$
CMRR	Op. Amp. Common Mode Rejection Ratio	42	60	80	—	dB	$V_{S0} = V_{CA-} = 0.1V$ & $5V$
PSRR	Op. Amp. Power Supply Rejection Ratio	43	55	75	—		$V_{S0} = V_{CA-} = 0.2V$ $V_{CC} = 10V$ & $20V$
$V_{OH,AMP}$	Op. Amp. High Level Output Voltage	44	5.0	5.2	5.4	V	$V_{CA-} = 0V$, $V_{S0} = 1V$
$V_{OL,AMP}$	Op. Amp. Low Level Output Voltage	45	—	—	20	mV	$V_{CA-} = 1V$, $V_{S0} = 0V$
$I_{SRC,AMP}$	Op. Amp. Output Source Current	46	2.3	4.0	—	mA	$V_{CA-} = 0V$, $V_{S0} = 1V$ $V_{CA0} = 4V$
$I_{SRC,AMP}$	Op. Amp. Output Sink Current	47	1.0	2.1	—		$V_{CA-} = 1V$, $V_{S0} = 0V$ $V_{CA0} = 2V$
$I_{O+,AMP}$	Operational Amplifier Output High Short Circuit Current	48	—	4.5	6.5		$V_{CA-} = 0V$, $V_{S0} = 5V$ $V_{CA0} = 0V$
$I_{O-,AMP}$	Operational Amplifier Output Low Short Circuit Current	49	—	3.2	5.2		$V_{CA-} = 5V$, $V_{S0} = 0V$ $V_{CA0} = 5V$

Lead Assignments



Functional Block Diagram



Lead Definitions

Symbol	Description
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
LIN1,2,3	Logic inputs for low side gate driver output (LO1,2,3), out of phase
FAULT	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
VCC	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
VSS	Logic ground
Vb1,2,3	High side floating supplies
HO1,2,3	High side gate drive outputs
Vs1,2,3	High side floating supply returns
LO1,2,3	Low side gate drive outputs
Vs0	Low side return and positive input of current amplifier

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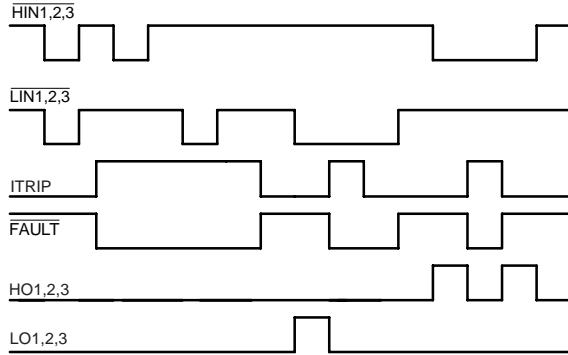


Figure 1. Input/Output Timing Diagram

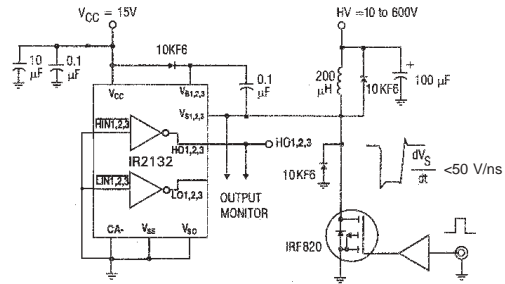


Figure 2. Floating Supply Voltage Transient Test Circuit

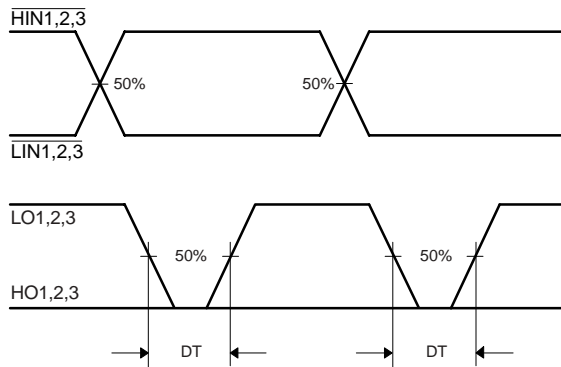


Figure 3. Deadtime Waveform Definitions

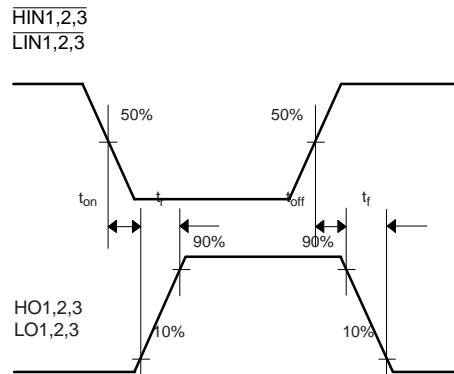


Figure 4. Input/Output Switching Time Waveform Definitions

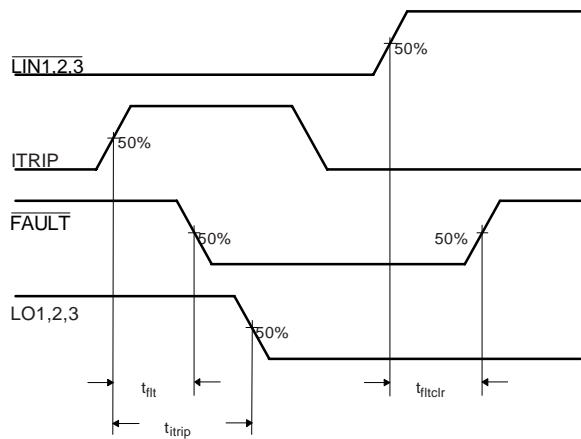


Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

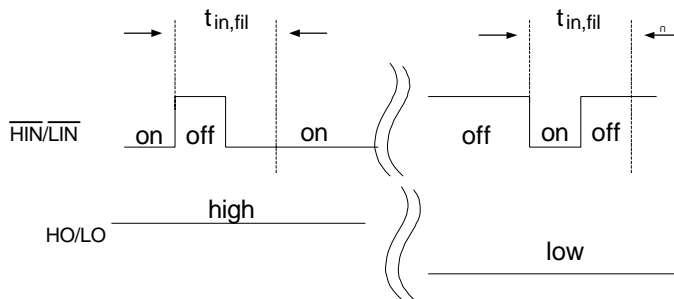


Figure 5.5 Input Filter Function

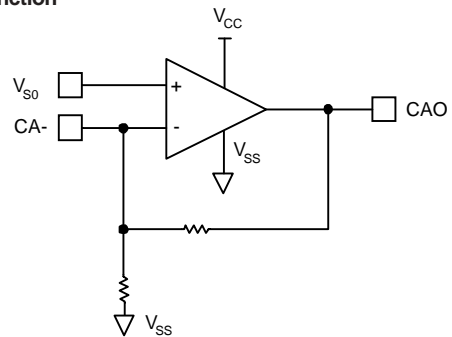


Figure 6. Diagnostic Feedback Operational Amplifier Circuit

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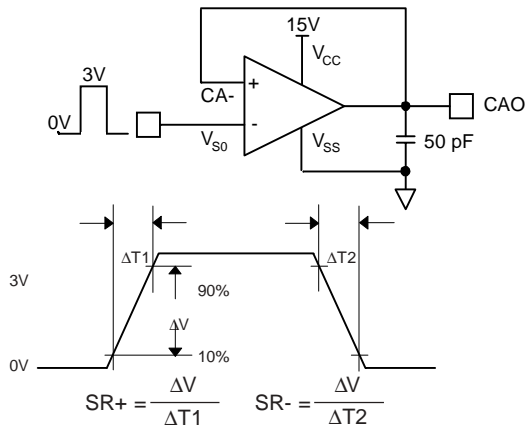


Figure 7. Operational Amplifier Slew Rate Measurement

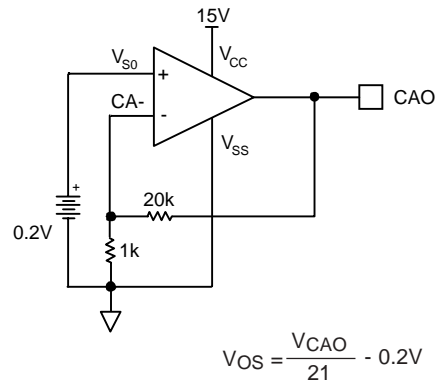


Figure 8. Operational Amplifier Input Offset Voltage Measurement

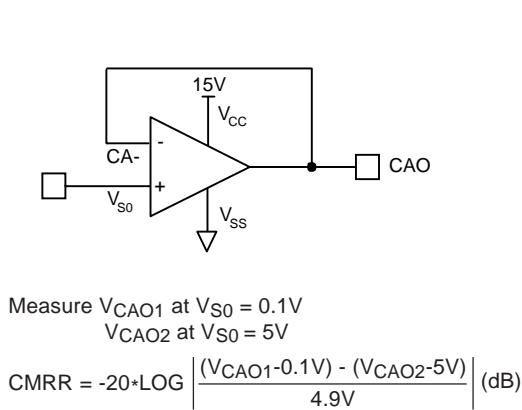


Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements

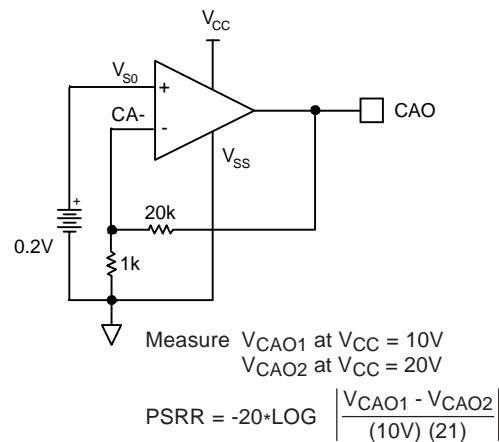
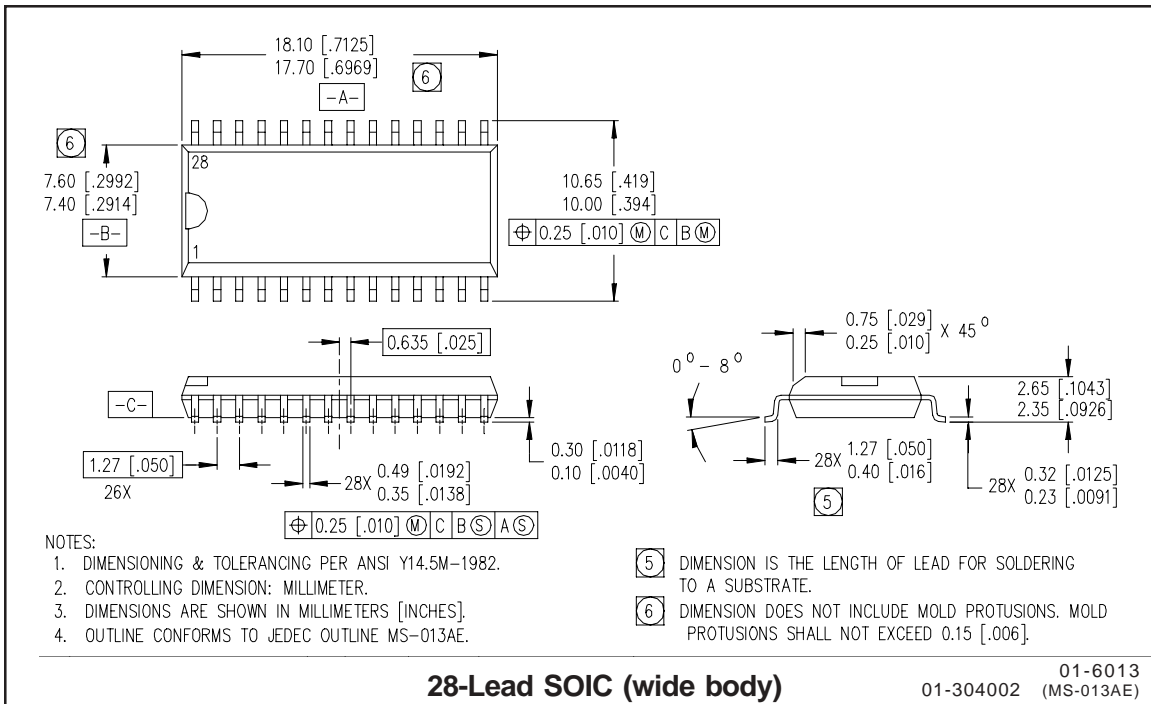
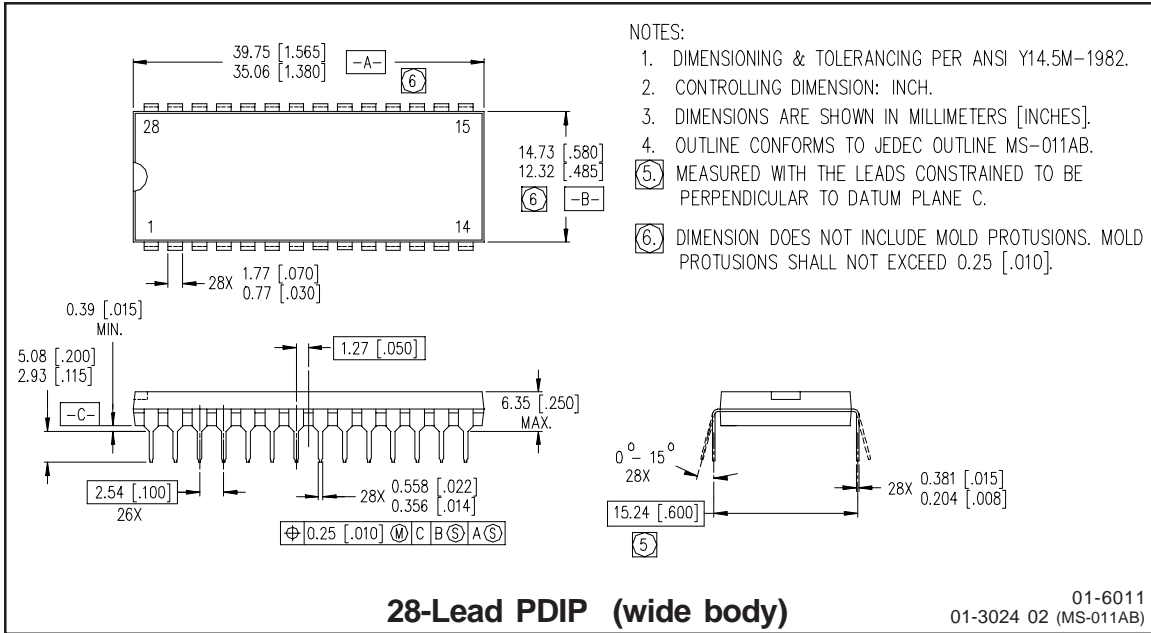


Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

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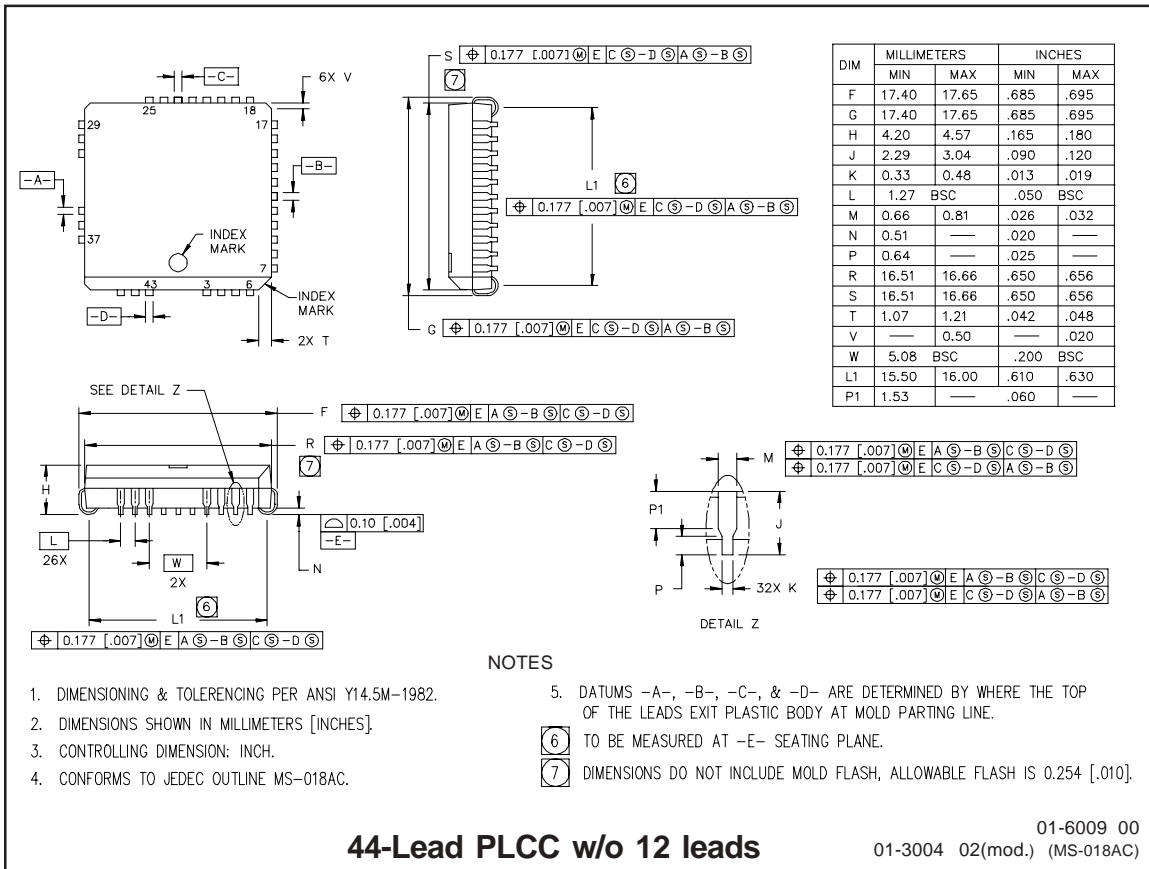
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Case outlines



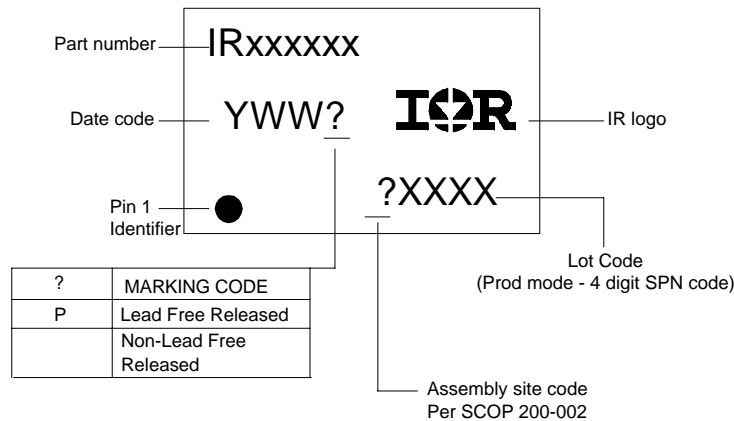
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Case outline



IR2130/IR2132(J)(S) & (PbF)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

28-Lead PDIP IR2130 order IR2130
 28-Lead SOIC IR2130S order IR2130S
 28-Lead PDIP IR2132 order IR2132
 28-Lead SOIC IR2132S order IR2132S
 44-Lead PLCC IR2130J order IR2130J
 44-Lead PLCC IR2132J order IR2132J

Leadfree Part

28-Lead PDIP IR2130 order IR2130PbF
 28-Lead SOIC IR2130S order IR2130SPbF
 28-Lead PDIP IR2132 order IR2132PbF
 28-Lead SOIC IR2132S order IR2132SPbF
 44-Lead PLCC IR2130J order IR2130JPbF
 44-Lead PLCC IR2132J order IR2132JPbF