FAIRCHILD

SEMICONDUCTOR®

March 2005

SPM™

FSBB20CH60
Smart Power Module

Features

- UL Certified No.E209204(SPM27-CA package)

- Very low thermal resistance due to using DBC

- 600V-20A 3-phase IGBT inverter bridge including control ICs for gate driving and protection

- Divided negative dc-link terminals for inverter current sensing applications

- Single-grounded power supply due to built-in HVIC

- Isolation rating of 2500Vrms/min.

Applications

- AC 100V ~ 253V three-phase inverter drive for small power ac motor drives

- Home appliances applications like air conditioner and washing machine.

General Description

It is an advanced smart power module (SPM™) that Fairchild has newly developed and designed to provide very compact and high performance ac motor drives mainly targeting low-power inverter-driven application like air conditioner and washing machine. It combines optimized circuit protection and drive matched to low-loss IGBTs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. The high speed built-in HVIC provides opto-coupler-less single-supply IGBT gate driving capability that further reduce the overall size of the inverter system design. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.
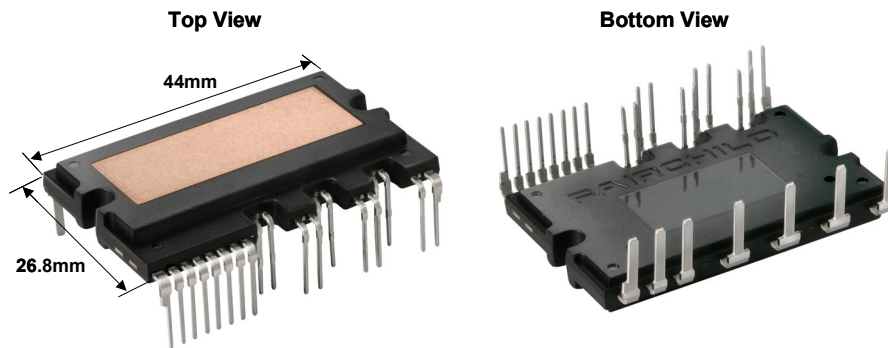
Top View

Bottom View

44mm

26.8mm

Figure 1.

www.fairchildsemi.com

Integrated Power Functions

• 600V-20A IGBT inverter for three-phase DC/AC power conversion (Please refer to Figure 3)

Integrated Drive, Protection and System Control Functions

• For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
　　　　　　　　　　　　　Control circuit under-voltage (UV) protection
　　　　　　　　　　　　　Note) Available bootstrap circuit example is given in Figures 10 and 11.

• For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
　　　　　　　　　　　　　Control supply circuit under-voltage (UV) protection

• Fault signaling: Corresponding to a UV fault (Low-side supply)

• Input interface: 3.3/5V CMOS/LSTTL compatible, Schmitt trigger input
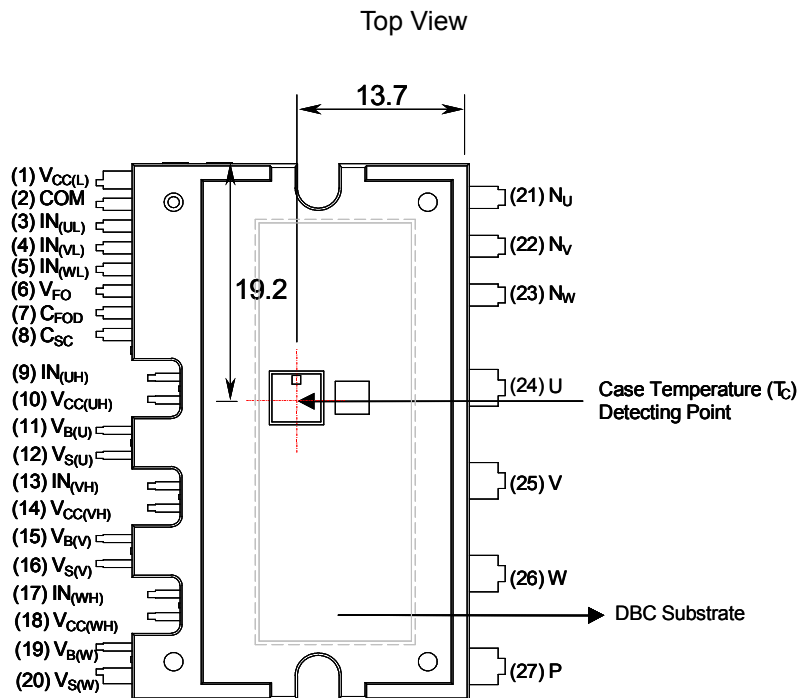
Pin Configuration

Top View

Figure 2.

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-side U Phase
10	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
11	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-side V Phase
14	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
15	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-side W Phase
18	$V_{CC(WH)}$	High-side Bias Voltage for W Phase IC
19	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC–Link Input for U Phase
22	N_V	Negative DC–Link Input for V Phase
23	N_W	Negative DC–Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC–Link Input

Internal Equivalent Circuit and Input/Output Pins
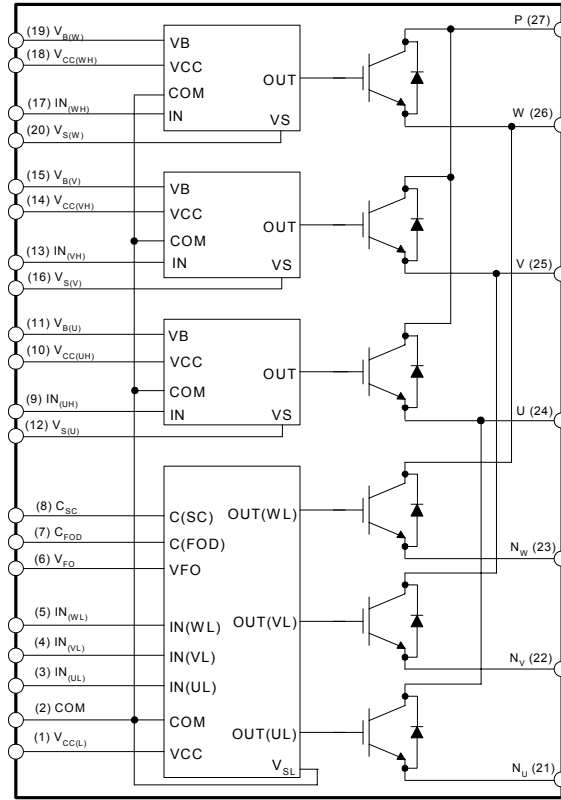
Note:

1. Inverter low-side is composed of three IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving and protection functions.

2. Inverter power side is composed of four inverter dc-link input terminals and three inverter output terminals.

3. Inverter high-side is composed of three IGBTs including freewheeling diodes (FWD) and three drive ICs for each IGBT.

Figure 3.

Absolute Maximum Ratings $(T_J = 25°C,$ Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	Supply Voltage	Applied between P- N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P- N_U, N_V, N_W	500	V
V_{CES}	Collector-emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	$T_C = 25°C$	20	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25°C$, Under 1ms Pulse Width	40	A
P_C	Collector Dissipation	$T_C = 25°C$ per One Chip	61	W
T_J	Operating Junction Temperature	(Note 1)	–20 ~ 125	°C

Note:

1. The maximum junction temperature rating of the power chips integrated within the SPM is 150 °C(@$T_C \leq 100°C$). However, to insure safe operation of the SPM, the average junction temperature should be limited to $T_{J(ave)} \leq 125°C$ (@$T_C \leq 100°C$)

Control Part

Symbol	Parameter	Conditions	Rating	Units
V_{CC}	Control Supply Voltage	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$, $V_{CC(L)}$ - COM	20	V
V_{BS}	High-side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	-0.3~17	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} - COM	-0.3~V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	5	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3~V_{CC}+0.3	V

Total System

Symbol	Parameter	Conditions	Rating	Units
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{CC} = V_{BS} = 13.5 \sim 16.5V$ $T_J = 125°C$, Non-repetitive, less than 2µs	400	V
T_C	Module Case Operation Temperature	-20°C$\leq T_J \leq$ 125°C, See Figure 2	-20 ~ 100	°C
T_{STG}	Storage Temperature		-40 ~ 125	°C
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, AC 1 minute, Connection Pins to ceramic substrate	2500	V_{rms}

Thermal Resistance

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Inverter IGBT part (per 1/6 module)	-	-	1.63	°C/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	-	-	2.55	°C/W

Note:

2. For the measurement point of case temperature(T_C), please refer to Figure 2.

Electrical Characteristics $(T_J = 25°C,$ Unless Otherwise Specified)

Inverter Part

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Units
$V_{CE(SAT)}$		Collector-Emitter Saturation Voltage	$V_{CC} = V_{BS} = 15V$ $V_{IN} = 5V$	$I_C = 20A, T_J = 25°C$	-	-	2.3	V
V_F		FWD Forward Voltage	$V_{IN} = 0V$	$I_C = 20A, T_J = 25°C$	-	-	2.1	V
HS	t_{ON}	Switching Times	$V_{PN} = 300V, V_{CC} = V_{BS} = 15V$ $I_C = 20A$ $V_{IN} = 0V \leftrightarrow 5V$, Inductive Load (Note 3)		-	0.48	-	us
	$t_{C(ON)}$				-	0.30	-	us
	t_{OFF}				-	0.93	-	us
	$t_{C(OFF)}$				-	0.52	-	us
	t_{rr}				-	0.10	-	us
LS	t_{ON}		$V_{PN} = 300V, V_{CC} = V_{BS} = 15V$ $I_C = 20A$ $V_{IN} = 0V \leftrightarrow 5V$, Inductive Load (Note 3)		-	0.63	-	us
	$t_{C(ON)}$				-	0.30	-	us
	t_{OFF}				-	1.01	-	us
	$t_{C(OFF)}$				-	0.51	-	us
	t_{rr}				-	0.10	-	us
	I_{CES}	Collector-Emitter Leakage Current	$V_{CE} = V_{CES}$		-	-	250	uA

Note:

3. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

(a) turn-on   **(b) turn-off**
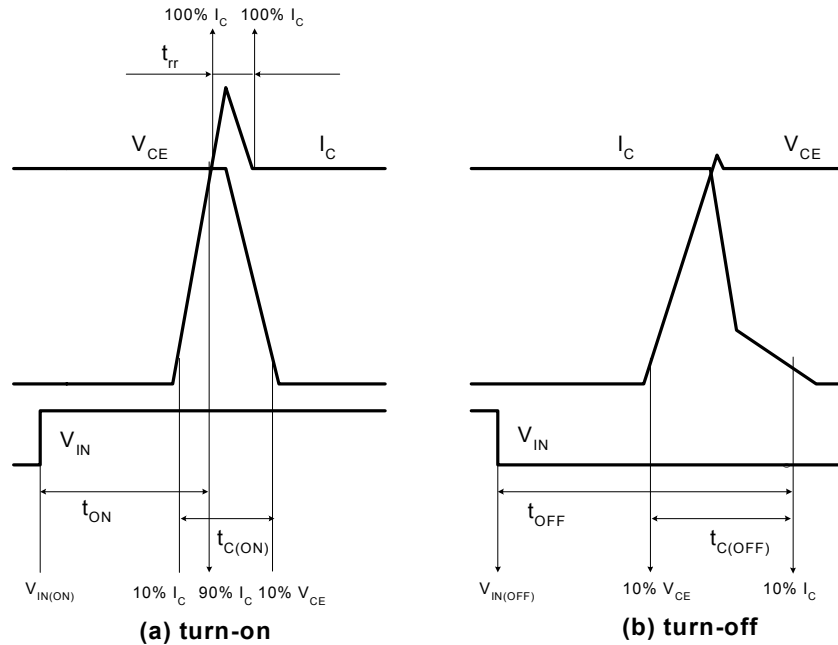
Figure 4. Switching Time Definition

Electrical Characteristics $(T_J = 25°C$, Unless Otherwise Specified)

Control Part

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
I_{QCCL}	Quiescent V_{CC} Supply Current	V_{CC} = 15V IN$_{(UL, VL, WL)}$ = 0V	$V_{CC(L)}$ - COM	-	-	23	mA
I_{QCCH}		V_{CC} = 15V IN$_{(UH, VH, WH)}$ = 0V	$V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$ - COM	-	-	100	uA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15V IN$_{(UH, VH, WH)}$ = 0V	$V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ -$V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	-	-	500	uA
V_{FOH}	Fault Output Voltage	V_{SC} = 0V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		4.5	-	-	V
V_{FOL}		V_{SC} = 1V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		-	-	0.8	V
$V_{SC(ref)}$	Short Circuit Trip Level	V_{CC} = 15V (Note 4)		0.45	0.5	0.55	V
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level		10.7	11.9	13.0	V
UV_{CCR}		Reset Level		11.2	12.4	13.2	V
UV_{BSD}		Detection Level		10.1	11.3	12.5	V
UV_{BSR}		Reset Level		10.5	11.7	12.9	V
t_{FOD}	Fault-out Pulse Width	C_{FOD} = 33nF (Note 5)		1.0	1.8	-	ms
$V_{IN(ON)}$	ON Threshold Voltage	Applied between IN$_{(UH)}$, IN$_{(VH)}$, IN$_{(WH)}$, IN$_{(UL)}$, IN$_{(VL)}$, IN$_{(WL)}$ - COM		3.0	-	-	V
$V_{IN(OFF)}$	OFF Threshold Voltage			-	-	0.8	V

Note:

4. Short-circuit current protection is functioning only at the low-sides.

5. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : C_{FOD} = 18.3 x 10^{-6} x t_{FOD}[F]

Recommended Operating Conditions

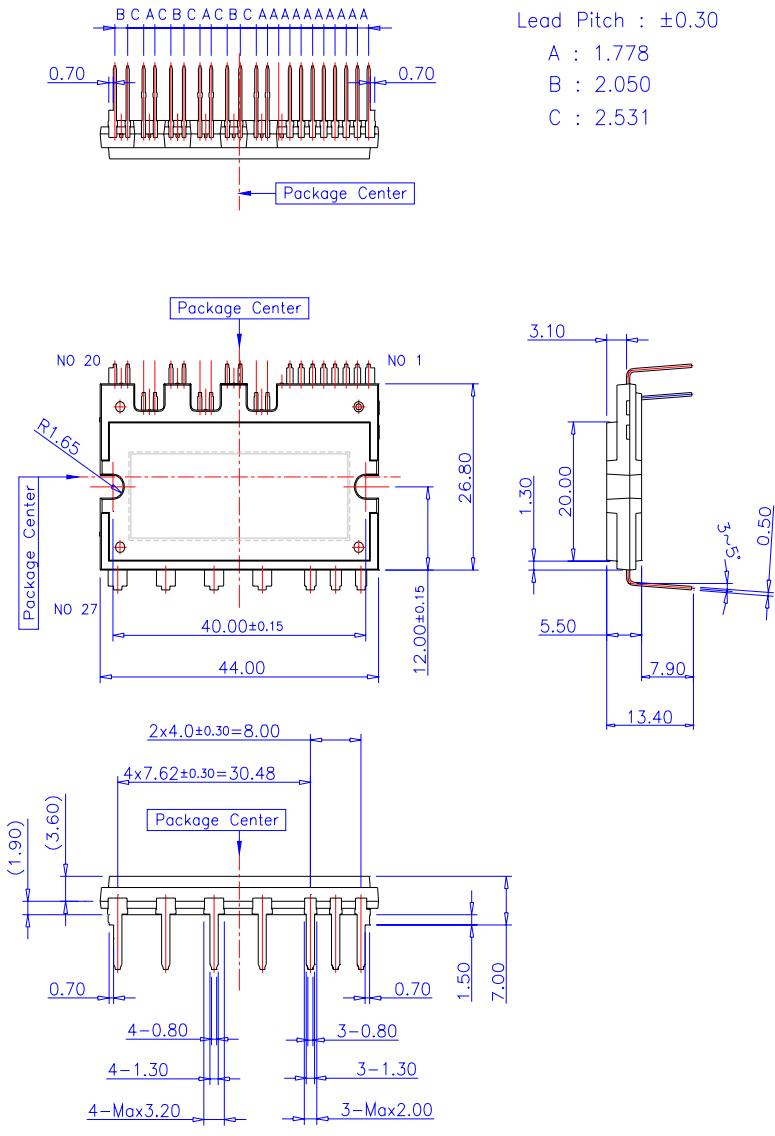| Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W	-	300	400	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$, $V_{CC(L)}$ - COM	13.5	15	16.5	V
V_{BS}	High-side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15	18.5	V
DV_{CC}/Dt, DV_{BS}/Dt	Control supply variation		-1	-	1	V/us
t_{dead}	Blanking Time for Preventing Arm-short	For Each Input Signal	2.5	-	-	us
f_{PWM}	PWM Input Signal	-20°C ≤ T_C ≤ 100°C, -20°C ≤ T_J ≤ 125°C	-	-	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W - COM (Including surge voltage)	-4		4	V

Mechanical Characteristics and Ratings

Parameter	Conditions		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: - M3	Recommended 0.62N•m	0.51	0.62	0.72	N•m
Device Flatness		Note Figure 5	0	-	+120	um
Weight			-	15.00	-	g
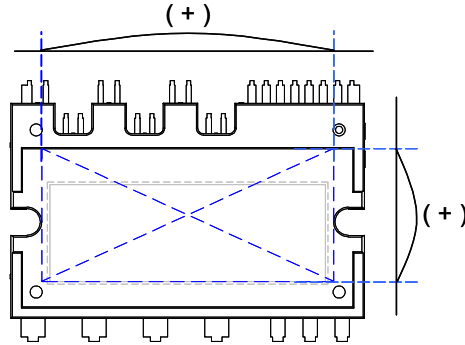
Figure 5. Flatness Measurement Position

Detailed Package Outline Drawings

Lead Pitch : ±0.30
A : 1.778
B : 2.050
C : 2.531

Detailed Package Outline Drawings (Continued)

30.60

26.50

R0.70

13.4

7.9

R0.70

Package Center

11.90±0.30

27.90±0.30

4.10±0.30
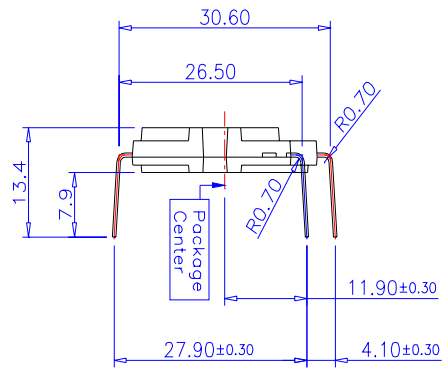
Lead Forming Dimension

Package Center

(2.306) (1.553)

Package Center

(2.76) (2.76)

19.694±0.30 20.447±0.30

19.24±0.30 19.24±0.30
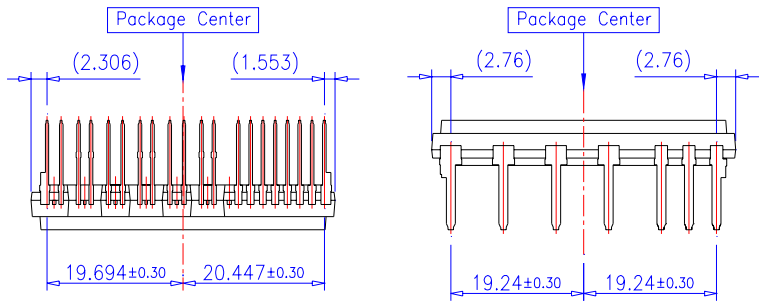
PKG Center to Lead Distance

FSBB20CH60 Rev. B

Detailed Package Outline Drawings (Continued)

DETAIL LEAD

LEAD TYPE 2

LEAD TYPE 3   LEAD TYPE 1

3.90±0.20

0.50±0.10   0.50±0.10   0.50±0.10

X   X'

MAX1.20   MAX0.70   MAX0.85

LEAD TYPE 1   LEAD TYPE 2   LEAD TYPE 3

SCALE 2 : 1

0.50   0.70   0.50

0.50   0.50   0.50

LEAD TYPE 1   LEAD TYPE 2   LEAD TYPE 3

SCALE 5 : 1

LEAD SECTION X-X'

FSBB20CH60 Rev. B

www.fairchildsemi.com