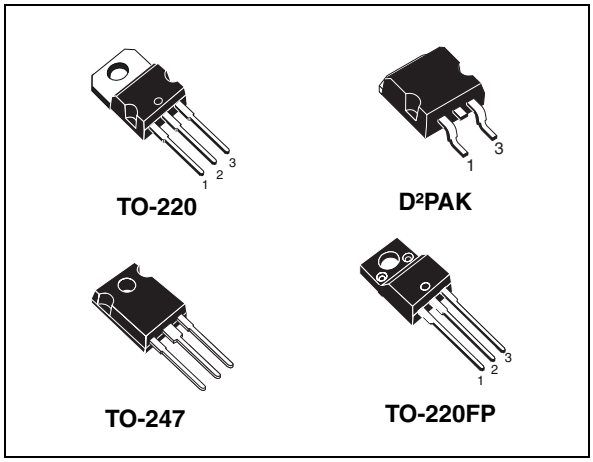
STB9NK90Z - STFPNK90Z
STP9NK90Z - STW9NK90Z

N-channel 900V - 1.1Ω - 8A - TO-220 /FP- D²PAK - TO-247
Zener-protected superMESH™ MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STB9NK90Z	900V	<1.3Ω	8A	160 W
STW9NK90Z	900V	<1.3Ω	8A	160 W
STP9NK90Z	900V	<1.3Ω	8A	160 W
STF9NK90Z	900V	<1.3Ω	8A	160 W

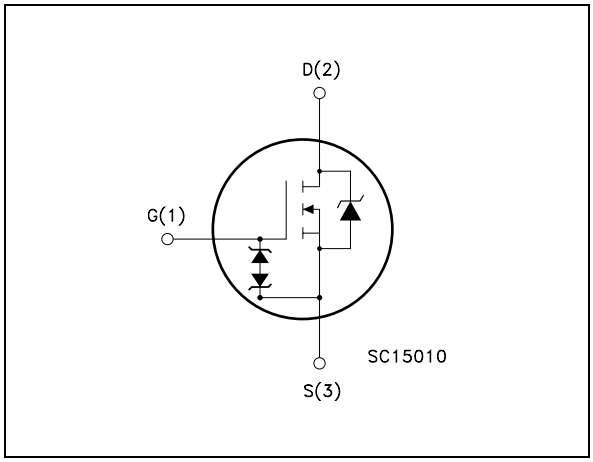
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STB9NK90Z	B9NK90Z	D²PAK	Tape & reel
STF9NK90Z	F9NK90Z	TO-220FP	Tube
STP9NK90Z	P9NK90Z	TO-220	Tube
STW9NK90Z	W9NK90Z	TO-247	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D²PAK/ TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	900		V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	900		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	8	8(1)	A
I_D	Drain current (continuous) at T_C=100°C	5	5(1)	A
I_{DM}(2)	Drain current (pulsed)	32	32(1)	A
P_{TOT}	Total dissipation at T_C = 25°C	160	40	W
	Derating Factor	1.28	0.32	W/°C
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5kΩ)	4		KV
dv/dt(3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (DC)	--	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 10A$, di/dt ≤200A/µs,$V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		TO-220 D²PAK	TO-20FP	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	0.78	3.1	0.78	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	62.5		50	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	8	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_d=I_{ar}, V_{DD}=50V)	300	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	900			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V, V_{DS} = 0			±10	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 100µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 3.6A		1.1	1.3	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 3.6 A		5.75		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		2115 190 40		pF pF pF
$C_{oss\ eq}$ (2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 720V		115		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=720V, I_D = 8A V_{GS} =10V (see Figure 19)		72 14 38		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise Time	V_{DD}=450 V, I_D=4A, R_G=4.7Ω, V_{GS}=10V (see Figure 20)		22 13		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=450 V, I_D=4A, R_G=4.7Ω, V_{GS}=10V (see Figure 20)		55 28		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD}=720 V, I_D=8A, R_G=4.7Ω, V_{GS}=10V (see Figure 20)		53 11 22		ns ns ns

Table 7. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO} (1)	Gate-Source Breakdown Voltage	Igs=±1mA (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				8	A
I_{SDM} (1)	Source-drain current (pulsed)				32	A
V_{SD} (2)	Forward on voltage	I_{SD}=8A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=8A, di/dt = 100A/µs, V_{DD}=50V, Tj=150°C		950 10 21		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%