CM200DX-24A

HIGH POWER SWITCHING USE

CM200DX-24A

- I_C 200A
- V_{CES} 1200V
- Dual

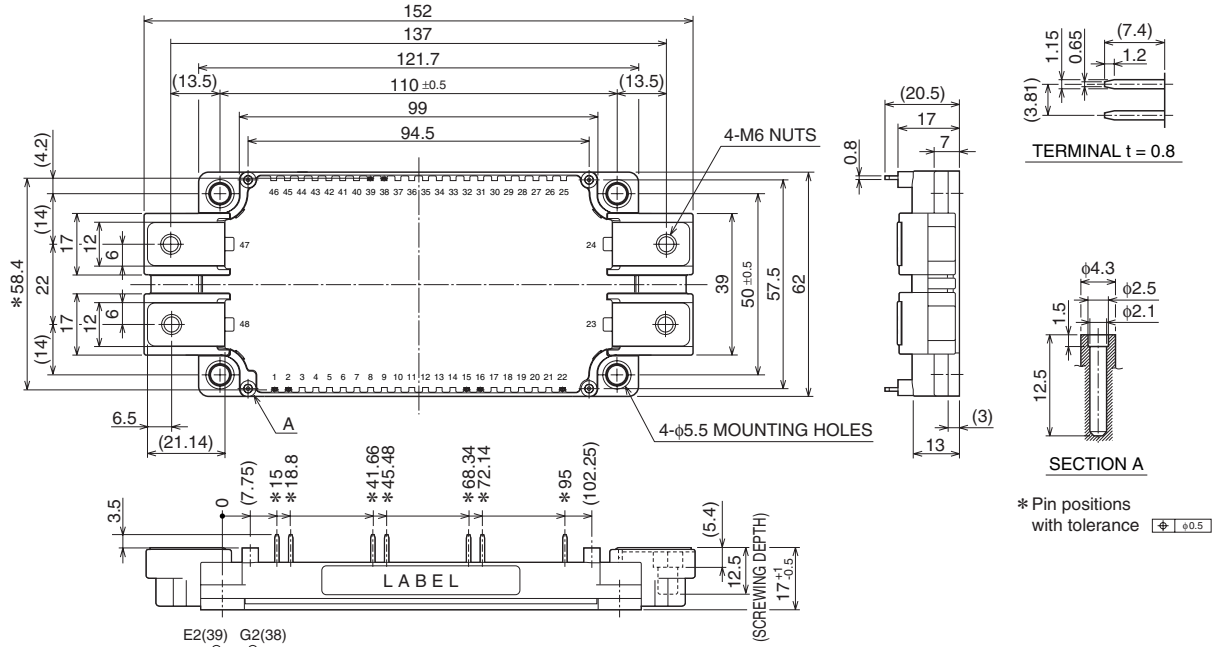
- Flatbase Type / Insulated Package / Copper (non-plating) base plate
- RoHS Directive compliant

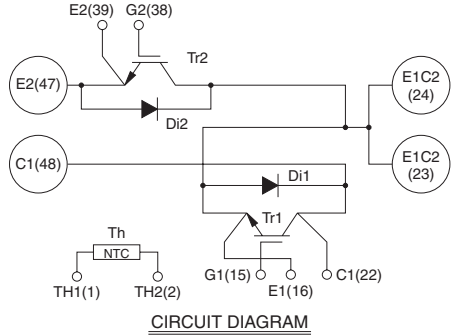
APPLICATION

General purpose Inverters, Servo Amplifiers, Power supply, etc.

OUTLINE DRAWING & CIRCUIT DIAGRAM

Dimensions in mm





CIRCUIT DIAGRAM

Tolerance otherwise specified

Division of Dimension	Tolerance
0.5 to 3	±0.2
over 3 to 6	±0.3
over 6 to 30	±0.5
over 30 to 120	±0.8
over 120 to 400	±1.2

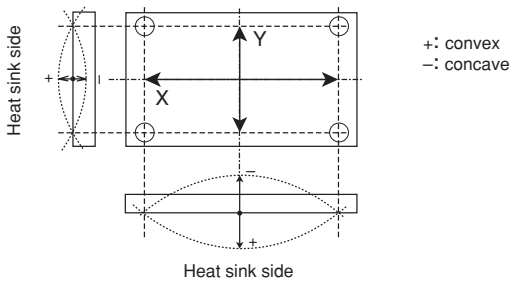
MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Tj = 25°C, unless otherwise specified)

INVERTER PART

Symbol	Parameter	Conditions	Rating	Unit
V_{CES}	Collector-emitter voltage	G-E Short	1200	V
V_{GES}	Gate-emitter voltage	C-E Short	±20	
I_C	Collector current	DC, T_C = 90°C (Note. 1)	200	A
I_{CRM}		Pulse (Note. 4)	400	
P_C	Maximum collector dissipation	T_C = 25°C (Note. 1, 5)	1250	W
I_E (Note.3)	Emitter current	T_C = 25°C (Note. 1)	200	A
I_{ERM}(Note.3)	(Free wheeling diode forward current)	Pulse (Note. 4)	400	
T_j	Junction temperature		–40 ~ +150	°C
T_{stg}	Storage temperature		–40 ~ +125	
V_{iso}	Isolation voltage	Terminals to base plate, f = 60Hz, AC 1 minute	2500	Vrms
—	Base plate flatness	On the centerilne X, Y (Note. 8)	±0 ~ +100	μm
—	Torque strength	Main terminals M6 screw	3.5 ~ 4.5	N·m
—	Torque strength	Mounting M5 screw	2.5 ~ 3.5	
—	Weight	(Typical)	330	g

Note. 8: The base plate flatness measurement points are in the following figure.



ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise specified)

INVERTER PART

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CES}	Collector cutoff current	V_{CE} = V_{CES}, V_{GE} = 0V		—	—	1	mA
$V_{GE(th)}$	Gate-emitter threshold voltage	I_C = 20mA, V_{CE} = 10V		6	7	8	V
I_{GES}	Gate leakage current	±V_{GE} = V_{GES}, V_{CE} = 0V		—	—	0.5	µA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 200A, V_{GE} = 15V (Note. 6)	T_j = 25°C	—	2.0	2.6	V
			T_j = 125°C	—	2.2	—	
		I_C = 200A, V_{GE} = 15V	Chip	—	1.9	—	
C_{ies}	Input capacitance	V_{CE} = 10V, V_{GE} = 0V (Note. 6)		—	—	35	nF
C_{oes}	Output capacitance			—	—	3.0	
C_{res}	Reverse transfer capacitance			—	—	0.68	
Q_G	Total gate charge	V_{CC} = 600V, I_C = 200A, V_{GE} = 15V		—	1000	—	nC
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600V, I_C = 200A		—	—	130	ns
t_r	Turn-on rise time	V_{GE} = ±15V, R_G = 1.6Ω		—	—	100	
$t_{d(off)}$	Turn-off delay time	Inductive load		—	—	450	
t_f	Turn-off fall time			—	—	600	
t_{rr} (Note.3)	Reverse recovery time	(I_E = 200A)		—	—	150	
Q_{rr} (Note.3)	Reverse recovery charge			—	8	—	µC
V_{EC}(Note.3)	Emitter-collector voltage	I_E = 200A, V_{GE} = 0V (Note. 6)	T_j = 25°C	—	2.6	3.4	V
			T_j = 125°C	—	2.16	—	
		I_E = 200A, V_{GE} = 0V	Chip	—	2.5	—	
R_{lead}	Module lead resistance	Main terminals-chip, per switch		—	1.6	—	mΩ
$R_{th(j-c)Q}$	Thermal resistance (Junction to case) (Note. 1)	per IGBT		—	—	0.10	K/W
$R_{th(j-c)R}$		per free wheeling diode		—	—	0.19	
$R_{th(c-f)}$	Contact thermal resistance (Case to heat sink) (Note. 1)	Thermal grease applied per 1 module (Note. 2)		—	0.015	—	
R_{Gint}	Internal gate resistance	T_C = 25°C, per switch		—	0	—	Ω
R_G	External gate resistance			1.6	—	16	

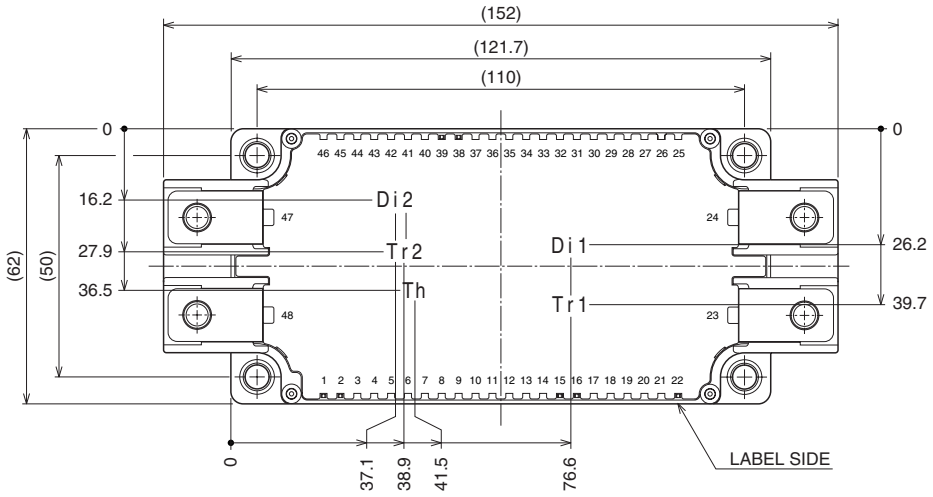
NTC THERMISTOR PART

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
R	Zero power resistance	T_C = 25°C	4.85	5.00	5.15	kΩ
ΔR/R	Deviation of resistance	T_C = 100°C, R_{100} = 493Ω	–7.3	—	+7.8	%
$B_{(25/50)}$	B constant	Approximate by equation (Note. 7)	—	3375	—	K
P_{25}	Power dissipation	T_C = 25°C	—	—	10	mW

Note.1: Case temperature (T_C), heat sink temperature (T_f) measured point is just under the chips. (Refer to the figure of the chip location.)
2: Typical value is measured by using thermally conductive grease of λ = 0.9W/(m·K).
3: I_E, I_{ERM}, V_{EC}, t_{rr} and Q_{rr} represent ratings and characteristics of the anti-parallel, emitter-collector free wheeling diode (FWDi).
4: Pulse width and repetition rate should be such that the device junction temperature (T_j) dose not exceed Tjmax rating.
5: Junction temperature (T_j) should not increase beyond 150°C.
6: Pulse width and repetition rate should be such as to cause negligible temperature rise.
(Refer to the figure of the test circuit for $V_{CE(sat)}$ and V_{EC})
7: $B_{(25/50)} = \ln(\frac{R_{25}}{R_{50}})/(\frac{1}{T_{25}} - \frac{1}{T_{50}})$
R_{25}: resistance at absolute temperature T_{25} [K]; T_{25} = 25 [°C]+273.15 = 298.15 [K]
R_{50}: resistance at absolute temperature T_{50} [K]; T_{50} = 50 [°C]+273.15 = 323.15 [K]

Chip Location (Top view)

Dimensions in mm (tolerance: ±1mm)



Each mark points the center position of each chip. Tr*: IGBT, Di*: FWDi, Th: NTC thermistor