VHF push-pull power MOS transistor BLF278

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Broadcast transmitters in the VHF frequency range.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 4-lead, SOT262A1 balanced flange package with two ceramic caps. The mounting flange provides the common source connection for the transistors.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

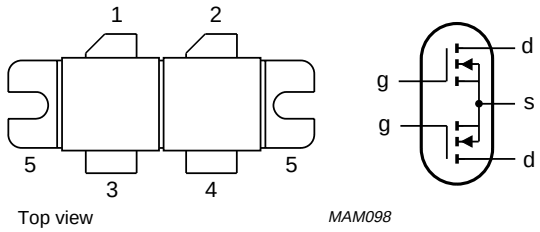


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	300	>20	>60
CW, class-C	108	50	300	typ. 18	typ. 80
CW, class-AB	225	50	250	>14 typ. 16	>50 typ. 55

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

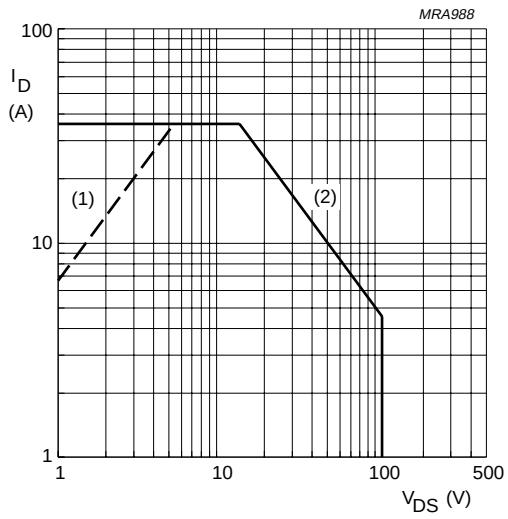
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section					
V_{DS}	drain-source voltage		–	125	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

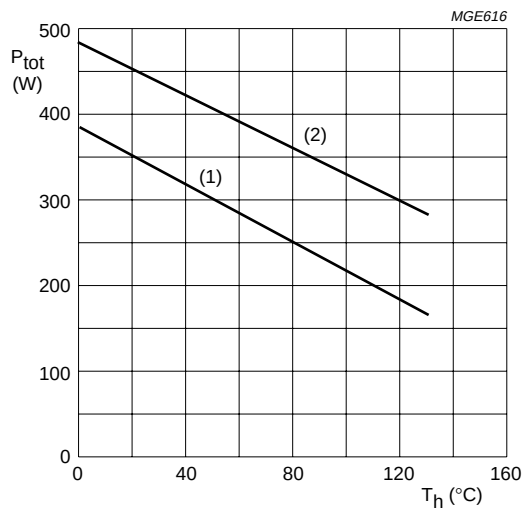
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	max. 0.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	max. 0.15	K/W



Total device; both sections equally loaded.
(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



Total device; both sections equally loaded.
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 100 mA	125	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	µA
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 50 mA	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both sections	V_{DS} = 10 V; I_D = 50 mA	–	–	100	mV
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both sections	V_{DS} = 10 V; I_D = 5 A	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0.2	0.3	Ω
I_{DSX}	drain cut-off current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF

V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			

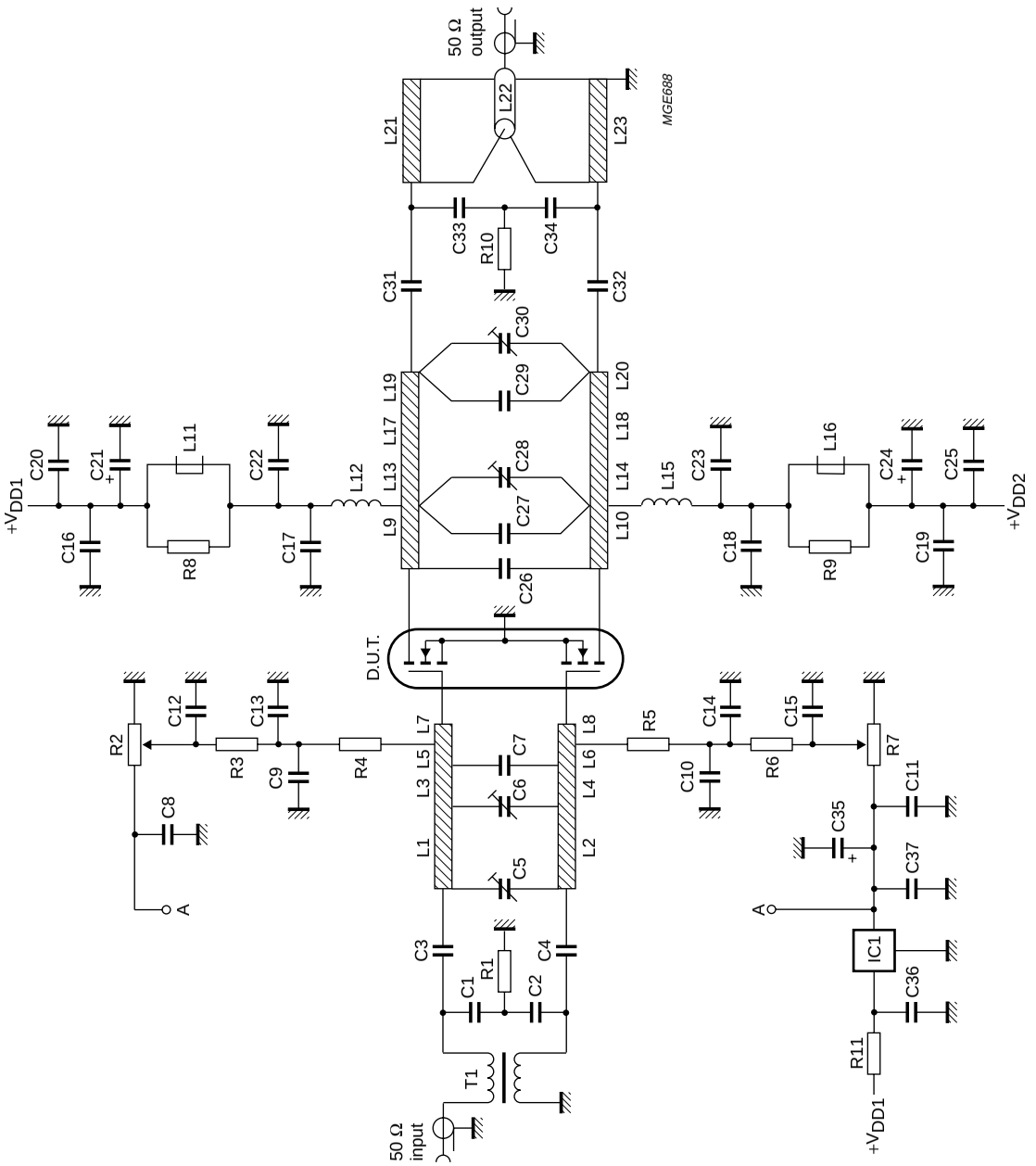


Fig.12 Class-B test circuit at f = 108 MHz.

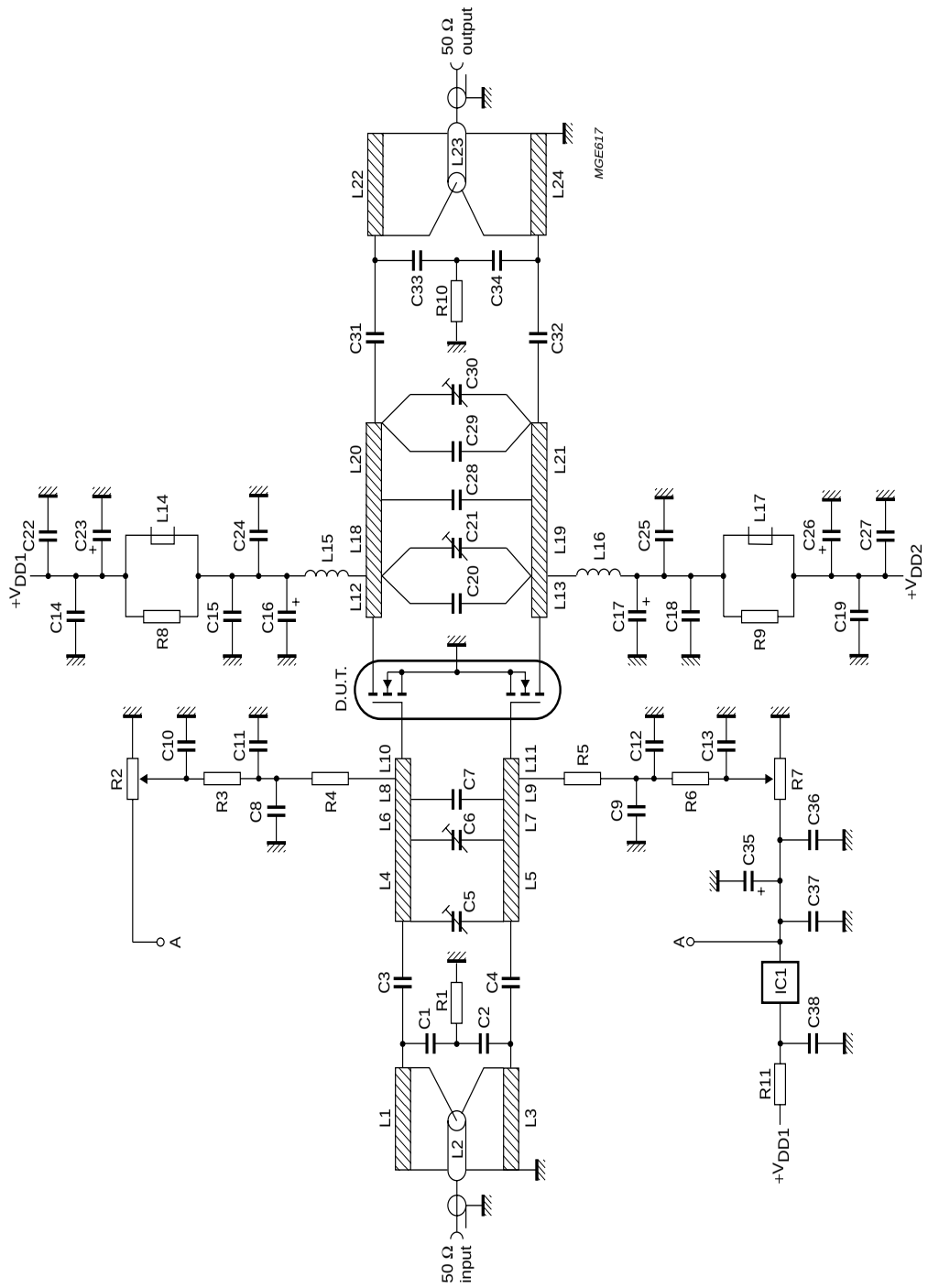
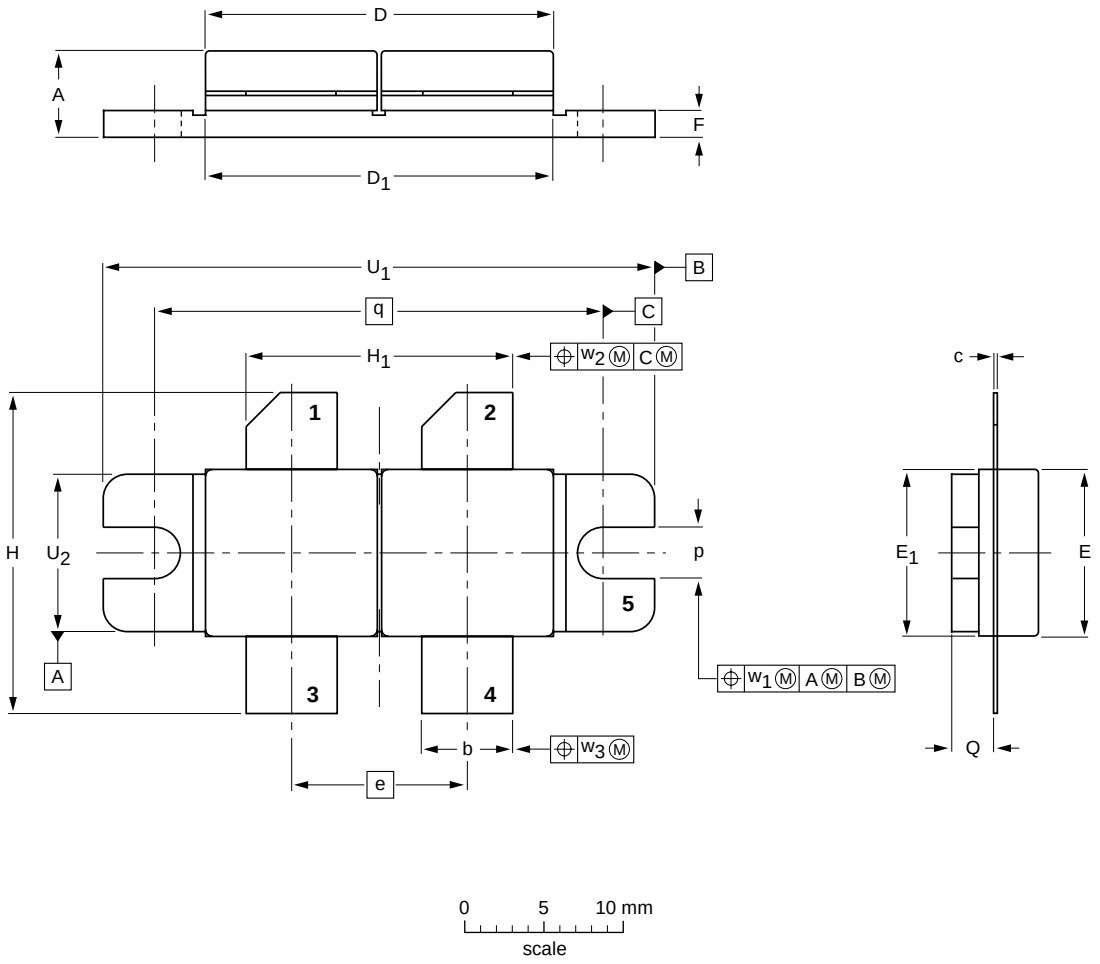


Fig.21 Class-AB test circuit at f = 225 MHz.

PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262A1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A1						99-03-29