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## FAST SWITCHING THYRISTOR

# ATF514

Repetitive voltage up to **1200 V**  
Mean on-state current **1100 A**  
Surge current **16 kA**  
Turn-off time **20 μs**

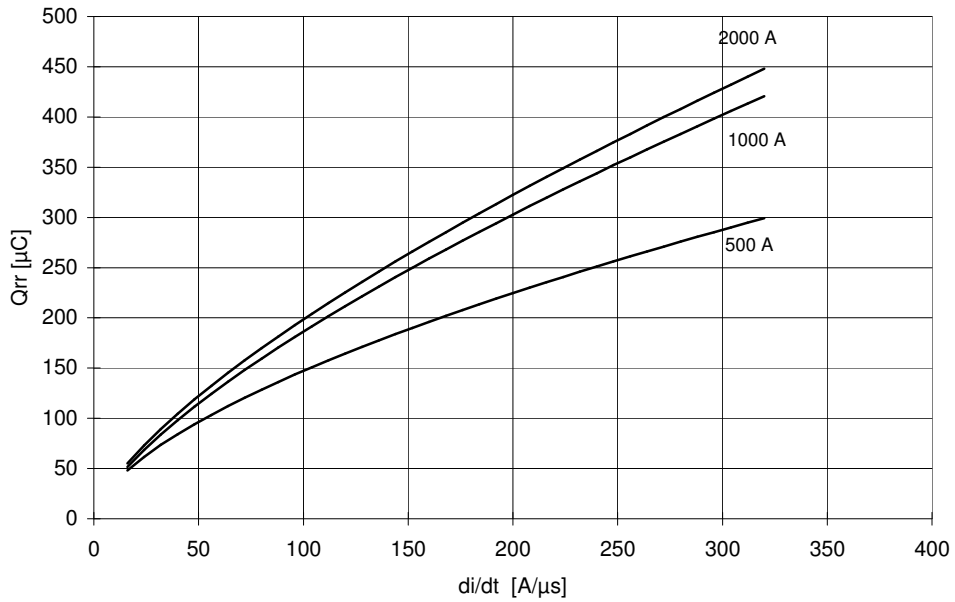
### FINAL SPECIFICATION

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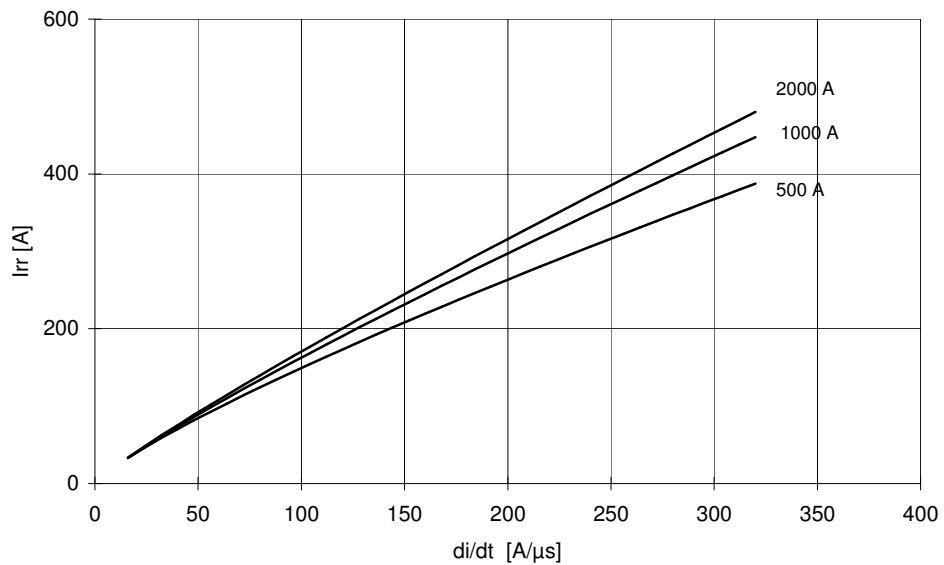
Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit															
<b>BLOCKING</b>																				
V <sub>RRM</sub>	Repetitive peak reverse voltage		125	1200	V															
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	1300	V															
V <sub>DRM</sub>	Repetitive peak off-state voltage		125	1200	V															
I <sub>RRM</sub>	Repetitive peak reverse current	V=VRRM	125	100	mA															
I <sub>DRM</sub>	Repetitive peak off-state current	V=VDRM	125	100	mA															
<b>CONDUCTING</b>																				
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		1100	A															
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 1 kHz, Th=55°C, double side cooled		1025	A															
I <sub>TSM</sub>	Surge on-state current, non repetitive	sine wave, 10 ms	125	16	kA															
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		1280 x1E3	A <sup>2</sup> s															
V <sub>T</sub>	On-state voltage	On-state current = 2000 A	25	2,5	V															
V <sub>T(TO)</sub>	Threshold voltage		125	1,50	V															
r <sub>T</sub>	On-state slope resistance		125	0,350	mohm															
<b>SWITCHING</b>																				
di/dt	Critical rate of rise of on-state current, min	From 75% VDRM up to 1200 A, gate 10V 5 ohm	125	500	A/μs															
dv/dt	Critical rate of rise of off-state voltage, min	Linear ramp up to 75% of VDRM	125	600	V/μs															
td	Gate controlled delay time, typical	VD=200V, gate source 20V, 10 ohm, tr=.5 μs	25	0,85	μs															
tq	Circuit commutated turn-off time	di/dt = 60 A/μs, I <sub>T</sub> = 1000 A dV/dt = 200 V/μs, up to 80% VDRM	125	20	μs															
Q <sub>rr</sub>	Reverse recovery charge	di/dt = 60 A/μs, I <sub>T</sub> = 1000 A	125	130	μC															
I <sub>rr</sub>	Peak reverse recovery current	VR = 50 V		105	A															
I <sub>H</sub>	Holding current, typical	VD=5V, gate open circuit	25		mA															
I <sub>L</sub>	Latching current, typical	VD=12V, tp=30μs	25		mA															
<b>GATE</b>																				
V <sub>GT</sub>	Gate trigger voltage	VD=5V	25	3,5	V															
I <sub>GT</sub>	Gate trigger current	VD=5V	25	350	mA															
V <sub>GD</sub>	Non-trigger gate voltage, min.	VD=VDRM	125	0,25	V															
V <sub>FGM</sub>	Peak gate voltage (forward)		25	30	V															
I <sub>FGM</sub>	Peak gate current		25	10	A															
V <sub>RGM</sub>	Peak gate voltage (reverse)		25	5	V															
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs	25	150	W															
P <sub>G(AV)</sub>	Average gate power dissipation		25	3	W															
<b>MOUNTING</b>																				
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		26	°C/kW															
T <sub>j</sub>	Operating junction temperature			-30 / 125	°C															
F	Mounting force			14.0 / 17.0	kN															
	Mass			500	g															
<b>ORDERING INFORMATION : ATF514 S 12 A</b> _____ tq code																				
standard specification _____ VDRM&VRRM/100																				
<table border="1"> <tr> <td>D 10 μs</td> <td>C 12 μs</td> <td>B 15 μs</td> <td>A 20 μs</td> <td>L 25 μs</td> </tr> <tr> <td>M 30 μs</td> <td>N 35 μs</td> <td>P 40 μs</td> <td>R 45 μs</td> <td>S 50 μs</td> </tr> <tr> <td>T 60 μs</td> <td>U 70 μs</td> <td>W 80 μs</td> <td>X 100μs</td> <td>Y 150μs</td> </tr> </table>						D 10 μs	C 12 μs	B 15 μs	A 20 μs	L 25 μs	M 30 μs	N 35 μs	P 40 μs	R 45 μs	S 50 μs	T 60 μs	U 70 μs	W 80 μs	X 100μs	Y 150μs
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## SWITCHING CHARACTERISTICS

REVERSE RECOVERY CHARGE  
 $T_j = 125\text{ }^\circ\text{C}$



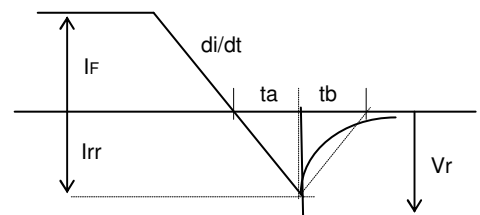
REVERSE RECOVERY CURRENT  
 $T_j = 125\text{ }^\circ\text{C}$



$$t_a = I_{rr} / (di/dt) \quad t_b = t_{rr} - t_a$$

$$\text{Softness (s factor)} \quad s = t_b / t_a$$

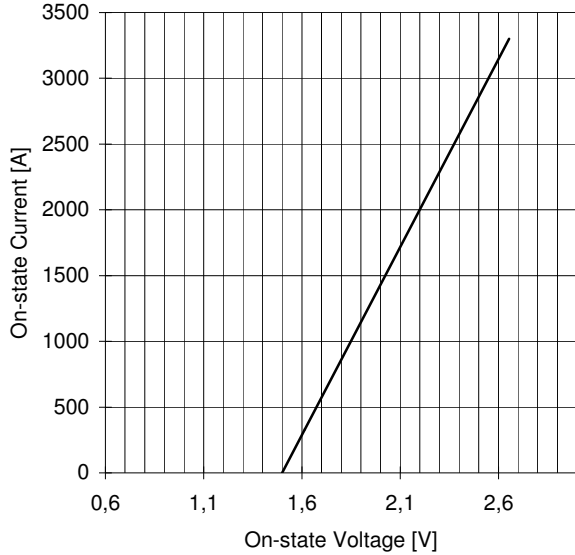
$$\text{Energy dissipation during recovery } E_r = V_r \cdot (Q_{rr} - I_{rr} \cdot t_a / 2)$$



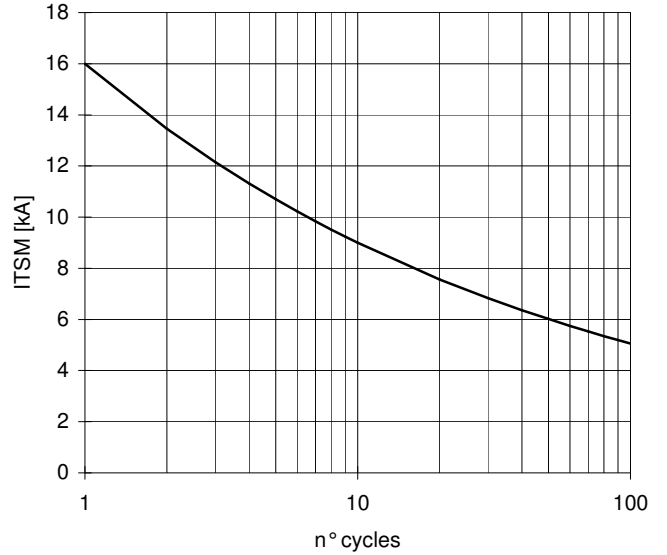
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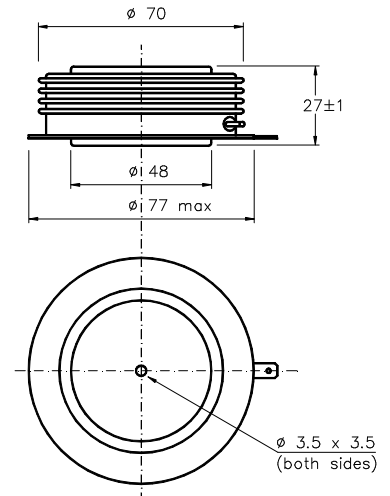
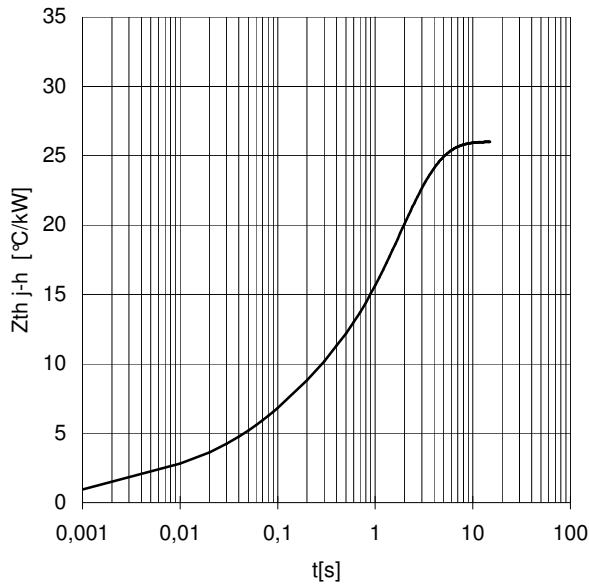
ON-STATE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



SURGE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE  
 DOUBLE SIDE COOLED



Cathode terminal type DIN 46244 - A 4.8 - 0.8  
 Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.  
 In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.  
 If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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