ANSALDO

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Tx 270318 ANSUSE I -

PHASE CONTROL THYRISTOR AT655

Repetitive voltage up to **2800 V**
Mean on-state current **1545 A**
Surge current **30 kA**

FINAL SPECIFICATION
feb 97 - ISSUE : 03

Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	2800	V
V_{RSM}	Non-repetitive peak reverse voltage		125	2900	V
V_{DRM}	Repetitive peak off-state voltage		125	2800	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	70	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	70	mA
CONDUCTING					
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		1545	A
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		1330	A
I_{TSM}	Surge on-state current	sine wave, 10 ms	125	30	kA
I^2t	I^2t	without reverse voltage		4500 x1E3	A^2s
V_T	On-state voltage	On-state current = 2900 A	25	1.8	V
$V_{T(TO)}$	Threshold voltage		125	1.05	V
r_T	On-state slope resistance		125	0.290	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 1730 A, gate 10V 5ohm	125	200	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	500	V/µs
td	Gate controlled delay time, typical	VD=100V, gate source 10V, 10 ohm , tr=.5 µs	25	3	µs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/µs linear up to 75% VDRM		320	µs
Q rr	Reverse recovery charge	di/dt=-20 A/µs, I= 1140 A	125		µC
I rr	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I_L	Latching current, typical	VD=5V, tp=30µs	25	700	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	3.5	V
I_{GT}	Gate trigger current	VD=5V	25	300	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0.25	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		21	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		6	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			22.0 / 24.5	kN
	Mass			520	g

ORDERING INFORMATION : AT655 S 28
standard specification — VDRM&VRRM/100

AT655 PHASE CONTROL THYRISTOR

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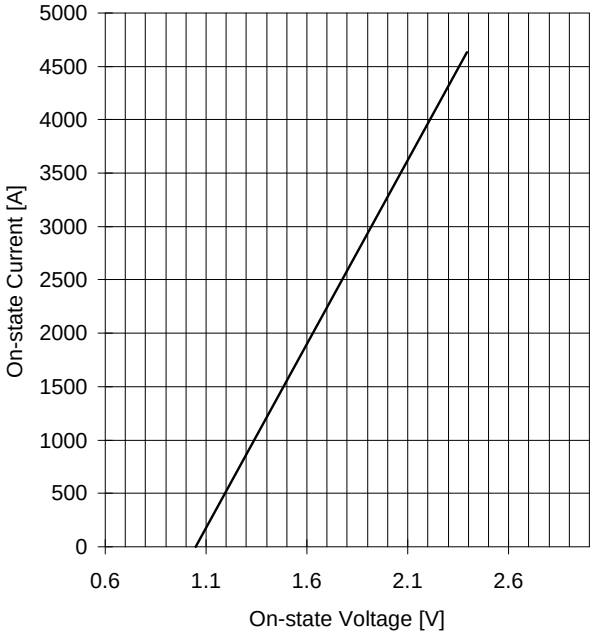
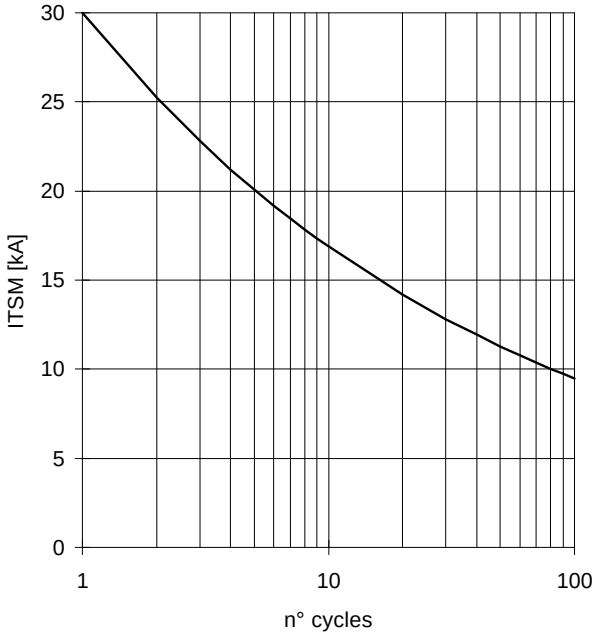
FINAL SPECIFICATION feb 97 - ISSUE : 03

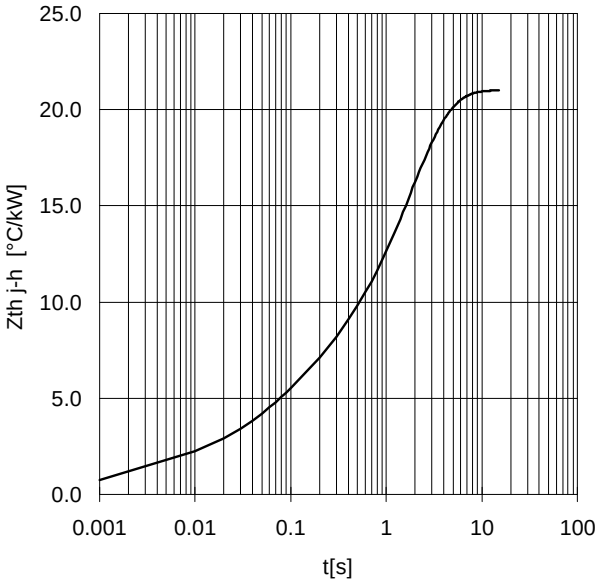
ON-STATE CHARACTERISTIC
Tj = 125 °C

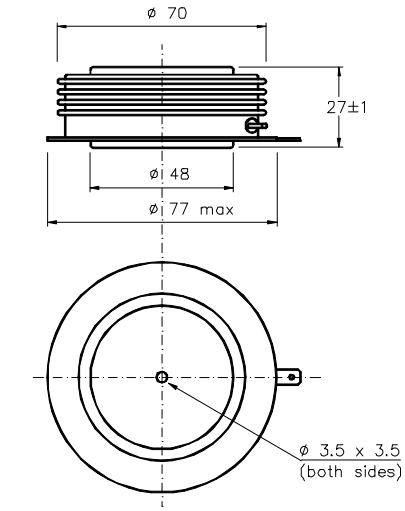


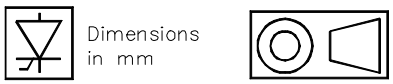
SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED







Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.

In the interest of product improvement ANSALDO reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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