SPECIFICATION

Device Name : IGBT - IPM

Type Name : 7MBP75RTB060

Spec. No. : MS6M 0653

Fuji Electric Co.,Ltd.
Matsumoto Factory

	DATE	NAME	APPROVED
DRAWN	Sep.- 17 -'02	K.Sekigawa	T.Fujihira
CHECKED	Sep. -17 -'02	Nishiura	
	Sep.-17 -'02	K.Yamada	

Fuji Electric Co.,Ltd.

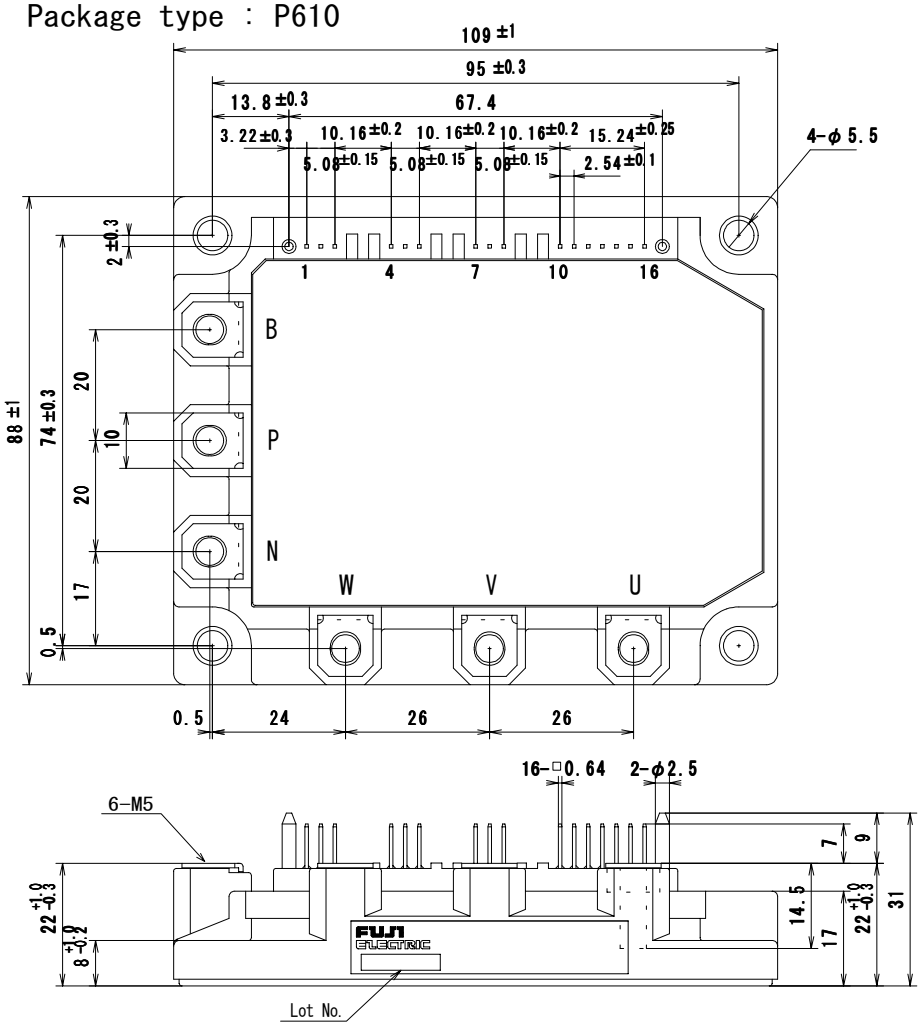
DWG.NO. MS6M 0653 1/23 a

Revised Records

Date	Classi-fication	Ind.	Content	Applied date	Drawn	Checked	Approved
Sep.-17-'02	enactment	——	————————	Issued date	K.Sekigawa	Nishiura K.Yamada	T.Fujihira
Apr.-09-'03	Revision	a	Reliability Test Items.	Apr.-09-'03	N.Matsuda	T.Miyasaka K.Yamada	T.Fujihira

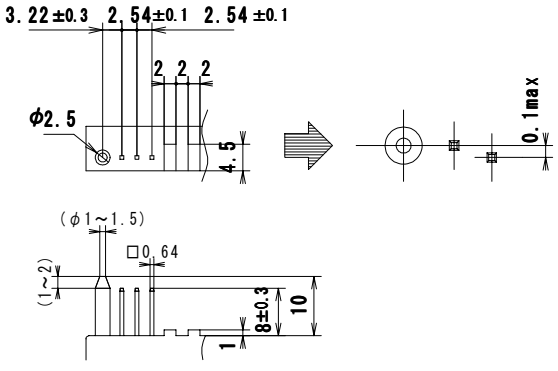
1. Outline Drawing (Unit : mm) ⓐ

Package type : P610



Indication of Lot No. □□□□□

- Odered No. in monthly
- Manufactured month (Jan.～Sep. :1～9, Oct. :O, Nov. :N, Dec. :D)
- Last digit of manufactured year



Details of control terminals

Dimensions in mm

2. Pin Descriptions

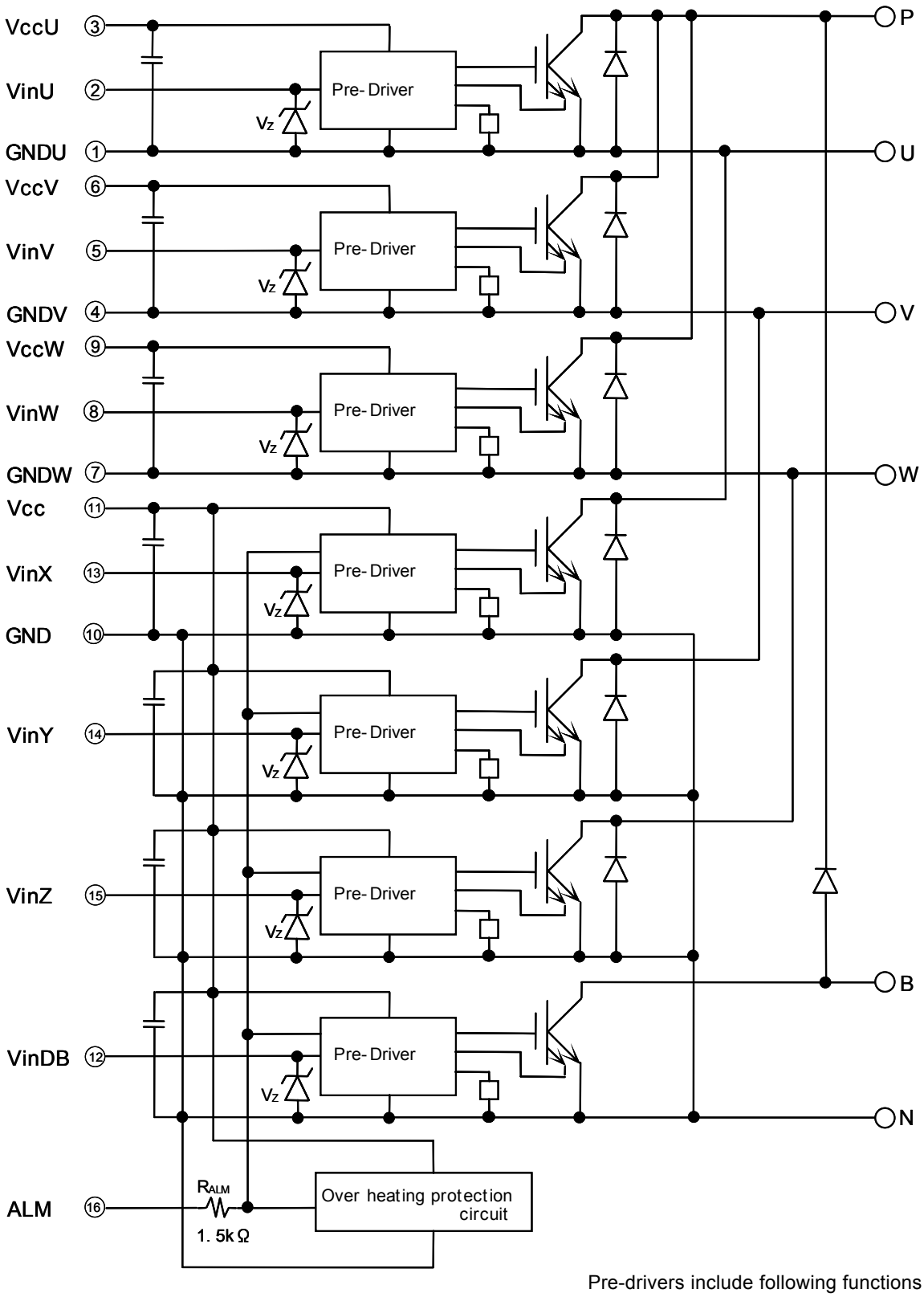
Main circuit

Symbol	Description
P	Positive input supply voltage.
U	Output (U).
V	Output (V).
W	Output (W).
N	Negative input supply voltage.
B	Collector terminal of Brake IGBT.

Control circuit

No.	Symbol	Description
①	GNDU	High side ground (U).
②	VinU	Logic input for IGBT gate drive (U).
③	VccU	High side supply voltage (U).
④	GNDV	High side ground (V).
⑤	VinV	Logic input for IGBT gate drive (V).
⑥	VccV	High side supply voltage (V).
⑦	GNDW	High side ground (W).
⑧	VinW	Logic input for IGBT gate drive (W).
⑨	VccW	High side supply voltage (W).
⑩	GND	Low side ground.
⑪	Vcc	Low side supply voltage.
⑫	VinDB	Logic input for Brake IGBT gate drive.
⑬	VinX	Logic input for IGBT gate drive (X).
⑭	VinY	Logic input for IGBT gate drive (Y).
⑮	VinZ	Logic input for IGBT gate drive (Z).
⑯	ALM	Low side alarm signal output.

3. Block Diagram



Pre-drivers include following functions

① Amplifier for driver
② Short circuit protection
③ Under voltage lockout circuit
④ Over current protection
⑤ IGBT chip over heating protection

4. Absolute Maximum Ratings

Tc＝25℃ unless otherwise specified.

Items			Symbol	Min.	Max.	Units
Bus Voltage (between terminal P and N)		DC	V_{DC}	0	450	V
		Surge	$V_{DC(surge)}$	0	500	V
		Shortoperating	Vsc	200	400	V
Collector-Emitter Voltage *1			Vces	0	600	V
Inverter	Collector Current	DC	Ic	-	75	A
		1ms	Icp	-	150	A
		Duty=75.0 % *2	-Ic	-	75	A
	Collector Power Dissipation	One transistor *3	Pc	-	198	W
Brake	Collector Current	DC	Ic	-	50	A
		1ms	Icp	-	100	A
	Forward Current of Diode		IF	-	50	A
	Collector Power Dissipation	One transistor *3	Pc	-	198	W
Supply Voltage of Pre-Driver *4			Vcc	-0.5	20	V
Input Signal Voltage *5			Vin	-0.5	Vcc+0.5	V
Input Signal Current			Iin	-	3	mA
Alarm Signal Voltage *6			VALM	-0.5	Vcc	V
Alarm Signal Current *7			IALM	-	20	mA
Junction Temperature			Tj	-	150	℃
Operating Case Temperature			Topr	-20	100	℃
Storage Temperature			Tstg	-40	125	℃
Isolating Voltage (Terminal to base, 50/60Hz sine wave 1min.) *8			Viso	-	AC2500	V
Screw Torque		Terminal (M5)	-	-	3.5	Nm
		Mounting (M5)				

Note

*1 : Vces shall be applied to the input voltage between terminal P and U or V or W or DB, N and U or V or W or DB

*2 : 125℃/FWD Rth(j-c)/(Ic×VF MAX)=125/0.855/(75×2.6)×100=75.0%

*3 : Pc=125℃/IGBT Rth(j-c)=125/0.63=198W [Inverter]
Pc=125℃/IGBT Rth(j-c)=125/0.63=198W [Break]

*4 : VCC shall be applied to the input voltage between terminal No.3 and 1,6 and 4, 9 and 7, 11 and 10.

*5 : Vin shall be applied to the input voltage between terminal No.2 and 1, 5 and 4, 8 and 7, 13,14,15 and 10.

*6 : VALM shall be applied to the voltage between terminal No.16 and 10.

*7 : IALM shall be applied to the input current to terminal No.16.

*8 : 50Hz/60Hz sine wave 1 minute.

5. Electrical Characteristics

Tj=25℃, Vcc=15V unless otherwise specified.

5.1 Main circuit

Item		Symbol	Conditions		Min.	Typ.	Max.	Units
Inverter	Collector Current at off signal input	I_{CES}	V_{CE}=600V Vin terminal open.		-	-	1.0	mA
	Collector-Emitter saturation voltage	$V_{CE(sat)}$	Ic=75A	Terminal	-	-	2.4	V
				Chip	-	2.0	-	V
	Forward voltage of FWD	VF	-Ic=75A	Terminal	-	-	2.6	V
				Chip	-	1.6	-	V
Brake	Collector Current at off signal input	I_{CES}	V_{CE}=600V Vin terminal open.		-	-	1.0	mA
	Collector-Emitter saturation voltage	$V_{CE(sat)}$	Ic=50A	Terminal	-	-	2.2	V
				Chip	-	1.75	-	V
	Forward voltage of Diode	VF	-Ic=50A	Terminal	-	-	3.3	V
				Chip	-	1.9	-	V
Turn-on time		ton	V_{DC}=300V、Tj=125℃		1.2	-	-	us
Turn-off time		toff	Ic=75A Fig.1, Fig.6		-	-	3.6	
Reverse recovery time		trr	V_{DC}=300V IF=75A Fig.1, Fig.6		-	-	0.3	
Maximum AvalancheEnergy (A non-repetition)		PAV	internal wiring inductance=50nH Main circuit wiring inductance=54nH		40	-	-	mJ

5.2 Control circuit

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply current of P-side pre-driver (one unit)	Iccp	Switching Frequency : 0～15kHz Tc=-20～125℃ Fig.7	-	-	18	mA
Supply current of N-side pre-driver	Iccn		-	-	65	mA
Input signal threshold voltage	Vin(th)	ON	1	1.35	1.7	V
		OFF	1.25	1.6	1.95	
Input Zener Voltage	Vz	Rin=20kΩ	-	8.0	-	V
Alarm Signal Hold Time	tALM	Tc=-20℃ Fig.2	1.1	-	-	ms
		Tc=25℃ Fig.2	-	2.0	-	
		Tc=125℃ Fig.2	-	-	4.0	
Current Limit Resistor	RALM	Alarm terminal	1425	1500	1575	Ω

5.3 Protection Section （Vcc＝15V）

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Over Current Protection Level of Inverter circuit	Ioc	Tj=125℃	113	-	-	A
Over Current Protection Level of Brake circuit		Tj=125℃	75	-	-	
Over Current Protection Delay time	tdoc	Tj=125℃	-	5	-	us
SC Protection Delay time	tsc	Tj=125℃ Fig.4	-	-	8	us
IGBT Chips Over Heating Protection Temperature Level	TjOH	Surface of IGBT Chips	150	-	-	℃
Over Heating Protection Hysteresis	TjH		-	20	-	℃
Over Heating Protection Temperature Level	TcOH	VDC=0V,IC=0A CaseTemperature	110	-	125	℃
Over Heating Protection Hysteresis	TcH		-	20	-	V
Under Voltage Protection Level	VUV		11	-	12.5	
Under Voltage Protection Hysteresis	VH		0.2	0.5	-	

6. Thermal Characteristics （Tc＝25℃）

Item			Symbol	Min.	Typ.	Max.	Units
Junction to Case Thermal Resistance *9	Inverter	IGBT	Rth(j-c)	-	-	0.63	℃/W
		FWD	Rth(j-c)	-	-	0.855	
	Brake	IGBT	Rth(j-c)			0.63	
Case to Fin Thermal Resistance with Compound			Rth(c-f)	-	0.05	-	

7. Noise Immunity （Vdc=300V、Vcc=15V、Test Circuit Fig 5.）

Item	Conditions	Min.	Typ.	Max.	Units
Common mode rectangular noise	Pulse width 1us,polarity ±,10 minuets Judge：no over-current, no miss operating	±2.0	-	-	kV
Common mode lightning surge	Rise time 1.2us,Fall time 50usInterval 20s,10 times Judge：no over-current, no miss operating	±5.0	-	-	kV

8. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
DC Bus Voltage	VDC	-	-	400	V
Power Supply Voltage of Pre-Driver	Vcc	13.5	15	16.5	V
Screw Torque (M5)	-	2.5	-	3	Nm

9. Weight

Item	Symbol	Min.	Typ.	Max.	Units
Weight	Wt	-	450	-	g

*9：(For 1device , Case is under the device)

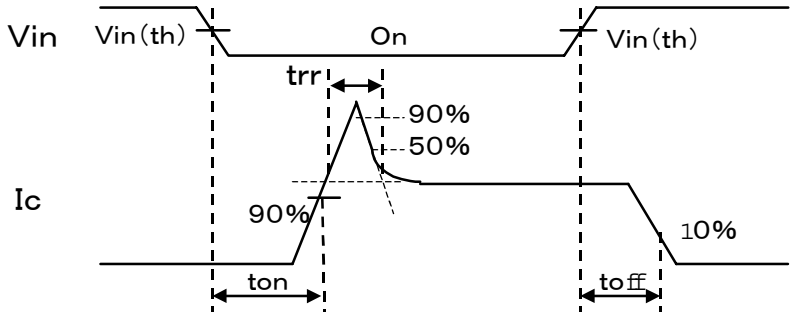


Figure 1. Switching Time Waveform Definitions

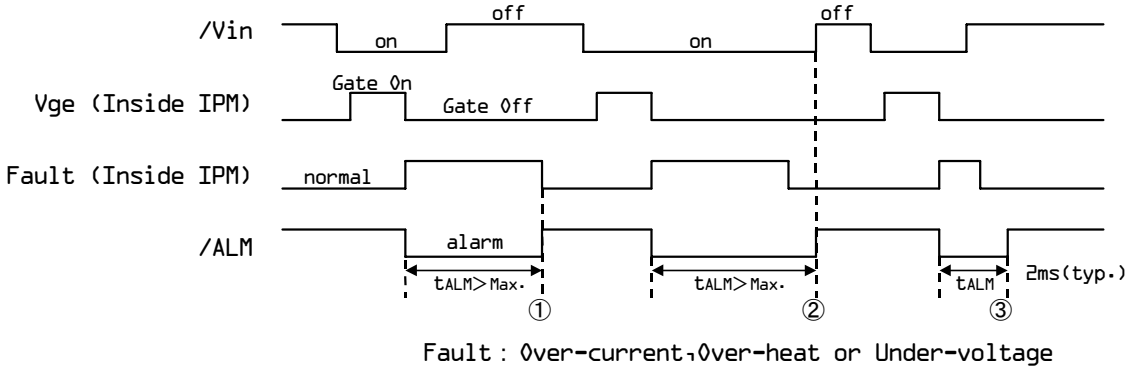


Figure 2. Input/Output Timing Diagram

Necessary conditions for alarm reset (refer to ① to ③ in figure2.)

① This represents the case when a failure-causing Fault lasts for a period more than tALM. The alarm resets when the input Vin is OFF and the Fault has disappeared.

② This represents the case when the ON condition of the input Vin lasts for a period more than tALM. The alarm resets when the Vin turns OFF under no Fault conditions.

③ This represents the case when the Fault disappears and the Vin turns OFF within tALM. The alarm resets after lasting for a period of the specified time tALM.

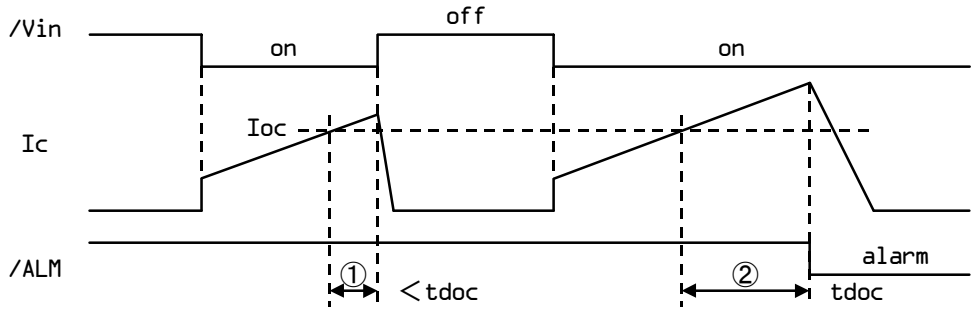


Figure 3. Over-current Protection Timing Diagram

Period ①: When a collector current over the OC level flows and the OFF command is input within a period less than the trip delay time tdoc, the current is hard-interrupted and no alarm is output.

Period ②: When a collector current over the OC level flows for a period more than the trip delay time tdoc, the current is soft-interrupted. If this is detected at the lower arm IGBTs, an alarm is output.

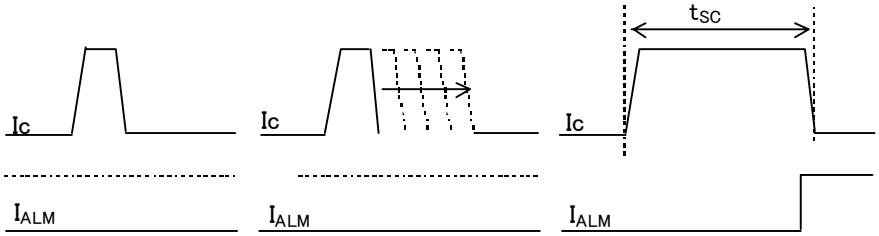


Figure.4 Definition of tsc

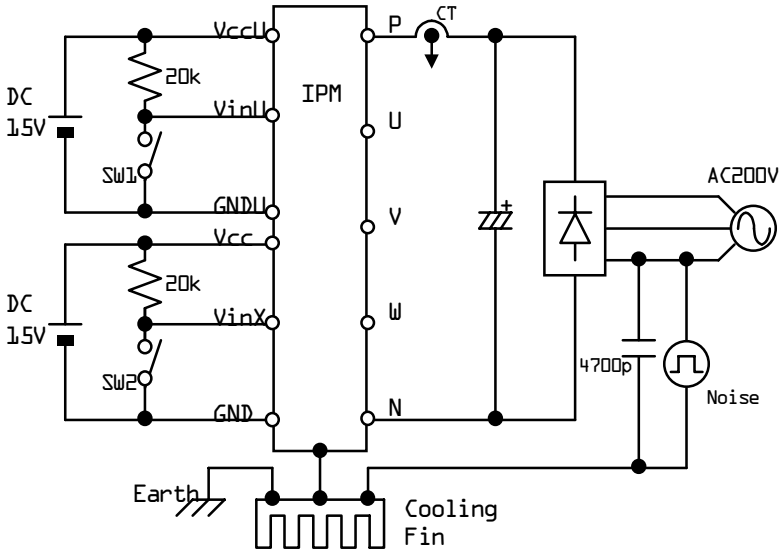


Figure 5. Noise Test Circuit

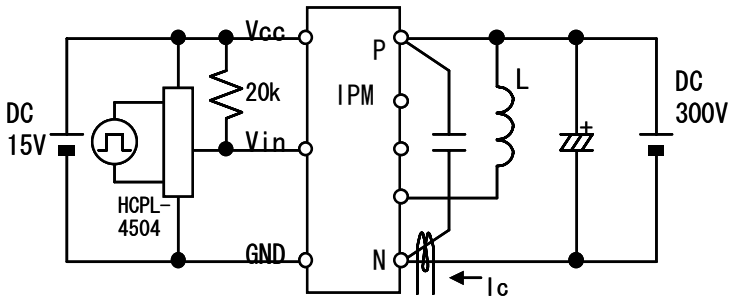


Figure 6. Switching Characteristics Test Circuit

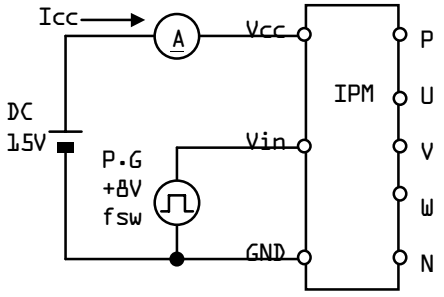


Figure 7. Icc Test Circuit

10. Truth table

10.1 IGBT Control

The following table shows the IGBT ON/OFF status with respect to the input signal Vin.

The IGBT turn-on when Vin is at “Low” level under no alarm condition.

Input (Vin)	Output (IGBT)
Low	ON
High	OFF

10.2 Fault Detection

(1) When a fault is detected at the high side, only the detected arm stops its output.
At that time the IPM dosen’t any alarm.

(2) When a fault is detected at the low side, all the lower arms stop their outputs and the IF
outputs an alarm of the low side.

	Fault	IGBT				Alarm Output
		U-phase	V-phase	W-phase	Low side	ALM
High side U-phase	OC	OFF	*	*	*	H
	UV	OFF	*	*	*	H
	TjOH	OFF	*	*	*	H
High side V-phase	OC	*	OFF	*	*	H
	UV	*	OFF	*	*	H
	TjOH	*	OFF	*	*	H
High side W-phase	OC	*	*	OFF	*	H
	UV	*	*	OFF	*	H
	TjOH	*	*	OFF	*	H
Low side	OC	*	*	*	OFF	L
	UV	*	*	*	OFF	L
	TjOH	*	*	*	OFF	L
Case Temperature	TcOH	*	*	*	OFF	L

*: Depend on input logic.

11. Cautions for design and application

1. Trace routing layout should be designed with particular attention to least stray capacity between the primary and secondary sides of optical isolators by minimizing the wiring length between the optical isolators and the IPM input terminals as possible.
   フォトカプラとIPMの入力端子間の配線は極力短くし、フォトカプラの一次側と二次側の浮遊容量を小さくしたパターンレイアウトにして下さい。

2. Mount a capacitor between Vcc and GND of each high-speed optical isolator as close to as possible.
   高速フォトカプラのVcc-GND間に、コンデンサを出来るだけ近接して取り付けて下さい。

3. For the high-speed optical isolator, use high-CMR type one with tpHL, tpLH ≦ 0.8μs.
   高速フォトカプラは、tpHL,tpLH≦0.8us、高CMRタイプをご使用ください。

4. For the alarm output circuit, use low-speed type optical isolators with CTR ≧ 100%.
   アラーム出力回路は、低速フォトカプラCTR≧100%のタイプをご使用ください。

5. For the control power Vcc, use four power supplies isolated each. And they should be designed to reduce the voltage variations.
   制御電源Vccは、絶縁された4電源を使用してください。また、電圧変動を抑えた設計として下さい。

6. Suppress surge voltages as possible by reducing the inductance between the DC bus P and N, and connecting some capacitors between the P and N terminals.
   P-N間の直流母線は出来るだけ低インダクタンス化し、P-N端子間にコンデンサを接続するなどしてサージ電圧を低減して下さい。

7. To prevent noise intrusion from the AC lines, connect a capacitor of some 4700pF between the three-phase lines each and the ground.
   ACラインからのノイズ侵入を防ぐために、3相各線－アース間に4700pF程のコンデンサを接続して下さい。

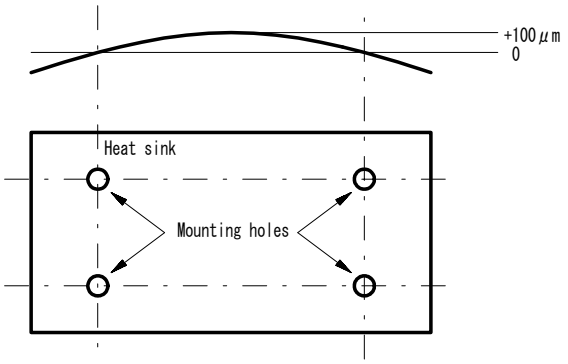
8. At the external circuit, never connect the control terminal ①GNDU to the main terminal U-phase, ④GNDV to V-phase, ⑦GNDW to W-phase, and ⑩GND to N-phase. Otherwise, malfunctions may be caused.
   制御端子①GNDUと主端子U相、制御端子④GNDVと主端子V相、制御端子⑦GNDWと主端子W相、制御端子⑩GNDと主端子Nを外部回路で接続しないで下さい。誤動作の原因になります。

9. Take note that an optical isolator's response to the primary input signal becomes slow if a capacitor is connected between the input terminal and GND.
   入力端子-GND間にコンデンサを接続すると、フォトカプラー次側入力信号に対する応答時間が長くなりますのでご注意ください。

10. Taking the used isolator's CTR into account, design with a sufficient allowance to decide the primary forward current of the optical isolator.
フォトカプラの一次側電流は、お使いのフォトカプラのCTRを考慮し十分に余裕をもった設計にして下さい。

11. Apply thermal compound to the surfaces between the IPM and its heat sink to reduce the thermal contact resistance.
接触熱抵抗を小さくするために、IPMとヒートシンクの間にサーマルコンパウンドを塗布して下さい。

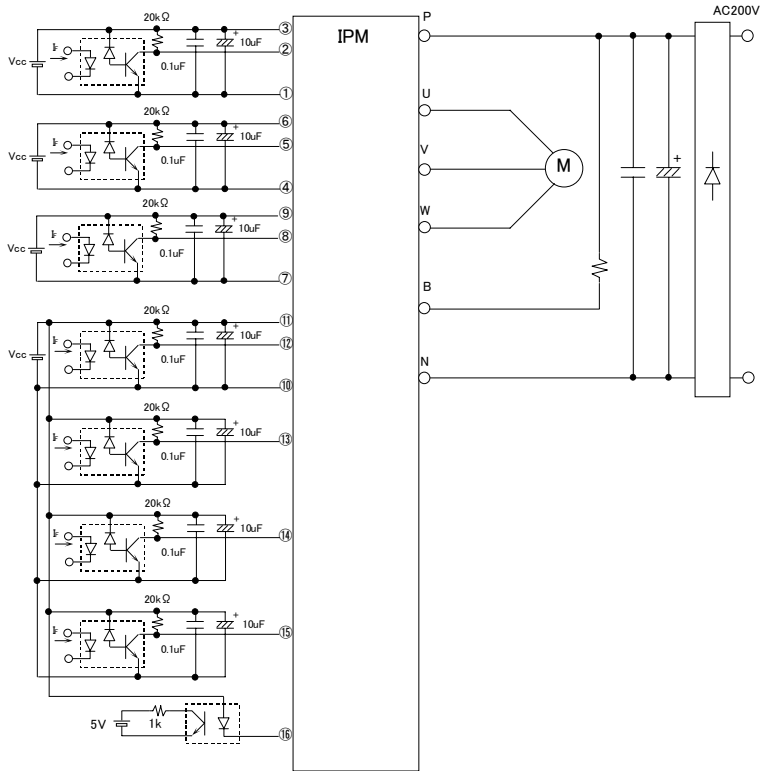
12. Finish the heat sink surface within roughness of 10μm and flatness (camber) between scre positions of 0 to +100μm. If the flatness is minus, the heat radiation becomes worse due to a gap between the heat sink and the IPM. And, if the flatness is over +100μm, there is a da that the IPM copper base may be deformed and this may cause a dielectric breakdown.
ヒートシンク表面の仕上げは、粗さ10um以下、ネジ位置間での平坦度(反り)は、0～100umとして下さい。平坦度がマイナスの場合、ヒートシンクとIPMの間に隙間ができ放熱が悪化します。また、平坦度が＋100um以上の場合IPMの銅ﾍﾞｰｽが変形し絶縁破壊を起こす危険性があります。



13. This product is designed on the assumption that it applies to an inverter use. Sufficient examination is required when applying to a converter use. Please contact Fuji Electric Co., if you would like to applying to converter use.
本製品は、インバータ用途への適用を前提に設計されております。コンバータ用途へ適用される場合は、十分な検討が必要です。もし、コンバータへ適用される場合は御連絡ください。

14. Please see the 『Fuji IGBT-IPM R SERIES APPLICATION MANUAL』 and 『Fuji IGBT MODULES N SERIES APPLICATION MANUAL』.
『富士IGBT-IPM Rシリーズ アプリケーションマニュアル』及び『IGBTﾓｼﾞｭｰﾙ Nシリーズ アプリケーションマニュアル』を御参照ください。

12. Example of applied circuit 応用回路例



13. Package and Marking 梱包仕様

Please see the MT6M4140 which is packing specification of P610 & P611 & P621 package.

P610, 611, 621 梱包仕様書 MT6M4140を御参照ください。

14. Cautions for storage and transportation 保管、運搬上の注意

- Store the modules at the normal temperature and humidity (5 to 35°C, 45 to 75%).
  常温常湿(5～35℃、45～75%)で保存して下さい。
- Avoid a sudden change in ambient temperature to prevent condensation on the module surfaces.
  モジュールの表面が結露しないよう、急激な温度変化を避けて下さい。
- Avoid places where corrosive gas generates or much dust exists.
  腐食性ガスの発生場所、粉塵の多い場所は避けて下さい。
- Store the module terminals under unprocessed conditions
  モジュールの端子は未加工の状態で保管すること。.
- Avoid physical shock or falls during the transportation.
  運搬時に衝撃を与えたり落下させないで下さい。

15. Scope of application 適用範囲

This specification is applied to the IGBT-IPM (type: 7MBP75RTB060).

本仕様書は、IGBT-IPM (型式:7MBP75RTB060)に適用する。

16. Based safety standards 準拠安全規格

UL1557