NEC

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR
2SK1492

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

PACKAGE DIMENSIONS
(in millimeters)

$\phi 3.0 \pm 0.2$
15.7 MAX.
4.7 MAX.
1.0
1.5
7.0
4
20.0 ± 0.2
6.0
4.5 ± 0.2
1 2 3
19 MIN.
3.2 ± 0.2
2.2 ± 0.2
1.0 ± 0.2
0.6 ± 0.1
2.8 ± 0.1
5.45
5.45

Drain

body diode

Gate

Gate protection diode

Source

1. Gate
2. Drain
3. Source
4. Fin (Drain)
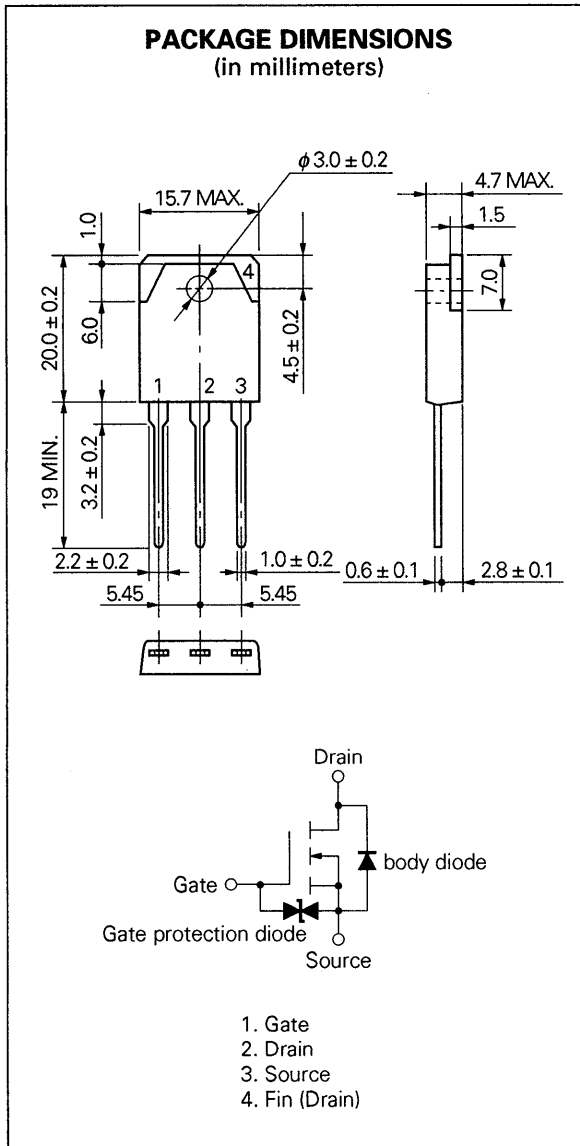
DESCRIPTION
The 2SK1492 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES
* Low On-state Resistance
    $R_{DS(on)} = 0.12 \ \Omega$ MAX. ($V_{GS} = 10$ V, $I_D = 18$ A)
* Low C_{iss} $C_{iss} = 3\ 000$ pF TYP.
* Built-in G-S Gate Protection Diodes
* High Avalanche Capability Ratings

QUALITY GRADE
Standard
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS
Maximum Temperatures

Storage Temperature		–55 to +150	°C
Channel Temperature		150 MAX.	°C

Maximum Power Dissipation

Total Power Dissipation ($T_a = 25$ °C)		140	W

Maximum Voltages and Currents ($T_a = 25$ °C)

V_{DSS}	Drain to Source Voltage	250	V
V_{GSS}	Gate to Source Voltage	±30	V
$I_{D(DC)}$	Drain Current (DC)	±35	A
$I_{D(pulse)}$*	Drain Current (pulse)	±140	A

* PW $\leq$ 10 μs, Duty Cycle $\leq$ 1 %

Maximum Avalanche Capability Ratings**

I_{AS}	Single Avalanche Current	52.5	A
E_{AS}	Single Avalanche Energy	2 500	mJ

**Starting $T_{ch} = 25$ °C, $R_G = 25$ Ω, $V_{GS} = 20$ V → 0

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.08	0.12	Ω	V_{GS} = 10 V, I_D = 18 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	7.0			S	V_{DS} = 10 V, I_D = 18 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 250 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		3 000		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		1 500		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		620		pF	f = 1 MHz
Turn-On Delay Time	$t_{d(on)}$		50		ns	V_{GS} = 10 V
Rise Time	t_r		240		ns	V_{DD} = 150 V
Turn-Off Delay Time	$t_{d(off)}$		140		ns	I_D = 18 A, R_G = 10 Ω
Fall Time	t_f		100		ns	R_L = 8.3 Ω
Total Gate Charge	Q_G		80		nC	V_{GS} = 10 V
Gate to Source Charge	Q_{GS}		17		nC	I_D = 35 A
Gate to Drain Charge	Q_{GD}		50		nC	V_{DD} = 200 V
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 35 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		370		ns	I_F = 35 A
Reverse Recovery Charge	Q_{rr}		2.8		μC	di/dt = 50 A/μs

Test Circuit 1: Avalanche Time
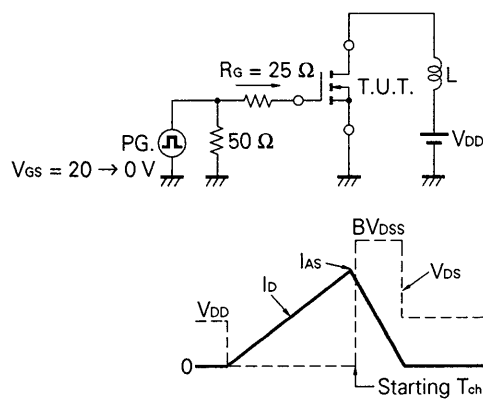
Test Circuit 2: Switching Time
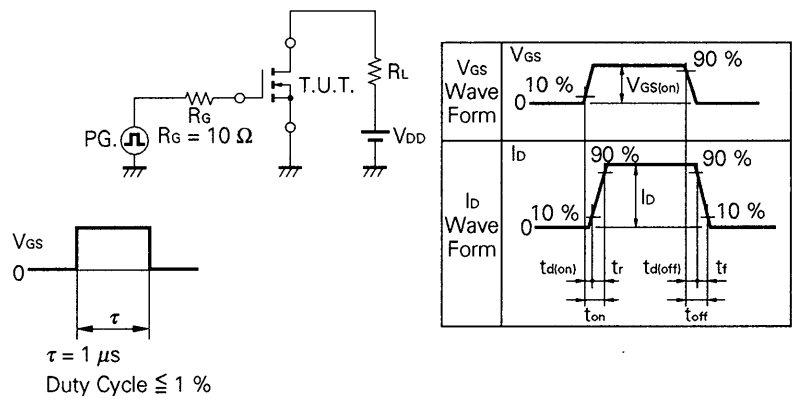
Test Circuit 3: Gate Charge